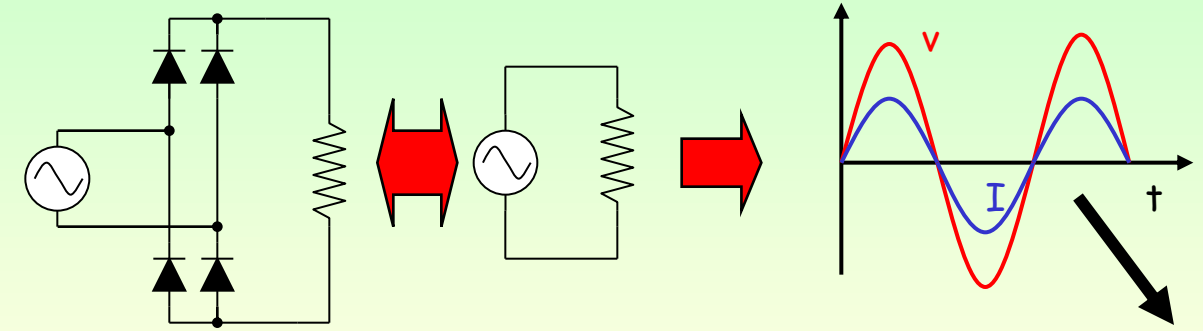
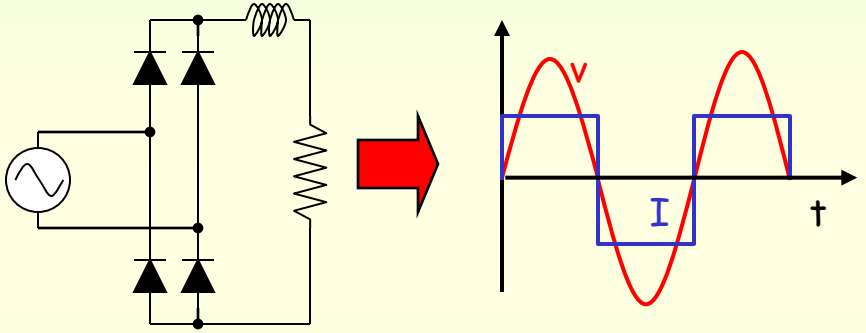
SISTEMAS ELECTRÓNICOS PARA ILUMINACIÓN

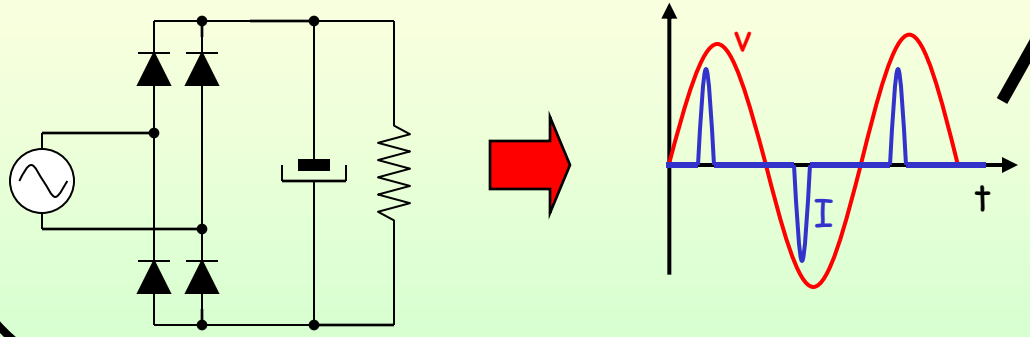
PARTE V: CORRECCIÓN DEL FACTOR DE POTENCIA

LOS BALASTOS ELECTRÓNICOS SON CARGAS NO LINEALES.

(FUENTE MUY IMPORTANTE DE INTERFERENCIAS)



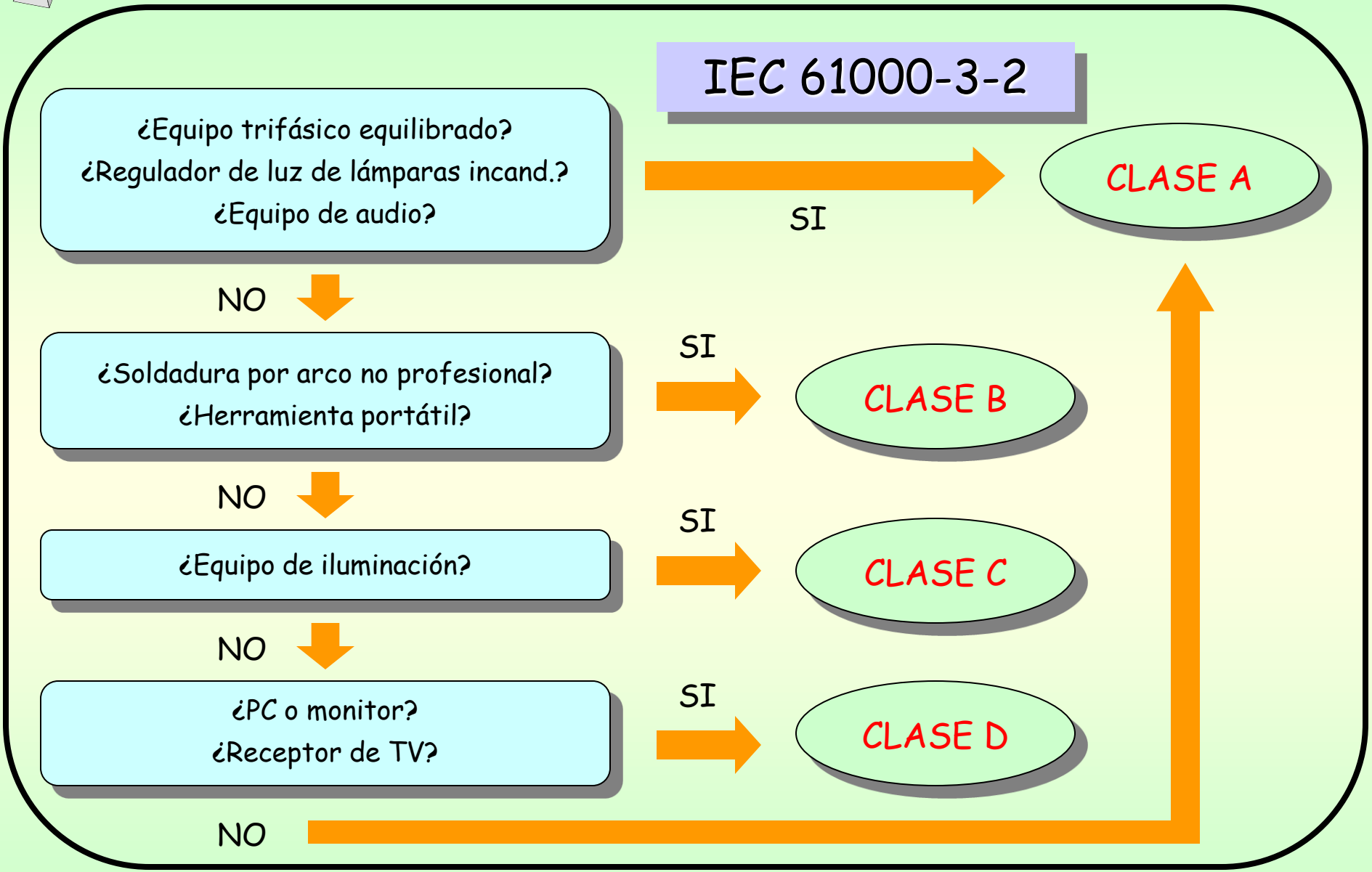




LA ETAPA DE ENTRADA DEL BALASTO ELECTRÓNICO TIENE UN EFECTO IMPORTANTE EN LA FORMA DE LA CORRIENTE

¡¡IMPORTANTE!!

LA CORRIENTE DEJA DE SER SENOIDAL


IEC 61000-3-2
¿Equipo trifásico equilibrado?
¿Regulador de luz de lámparas incand.?
¿Equipo de audio?
SI
CLASE A
NO
¿Soldadura por arco no profesional?
¿Herramienta portátil?
SI
CLASE B
NO
¿Equipo de iluminación?
SI
CLASE C
NO
¿PC o monitor?
¿Receptor de TV?
SI
CLASE D
NO

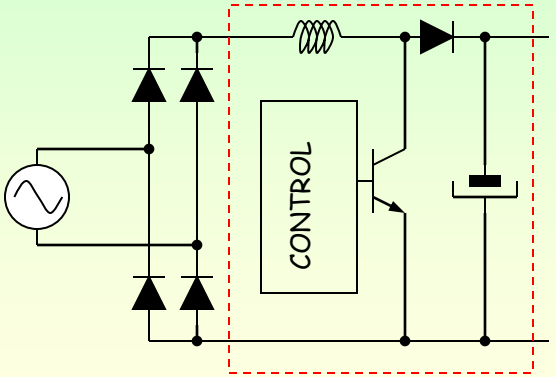
Límites armónicos impuestos por la norma IEC 61000-3-2 Clase C (Equipos de Iluminación)

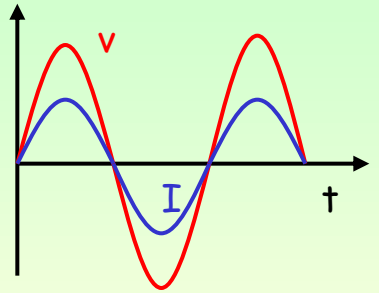
Tabla 2
Límites para equipos de Clase C

Orden del armónico n	Corriente armónica máxima admisible expresada en porcentaje de la corriente de entrada a la frecuencia fundamental %
2	2
3	30·λ*
5	10
7	7
9	5
$11 \leq n \leq 39$ (sólo armónicos impares)	3

* λ es el factor de potencia del circuito.

Elevador (BOOST)
como PFC

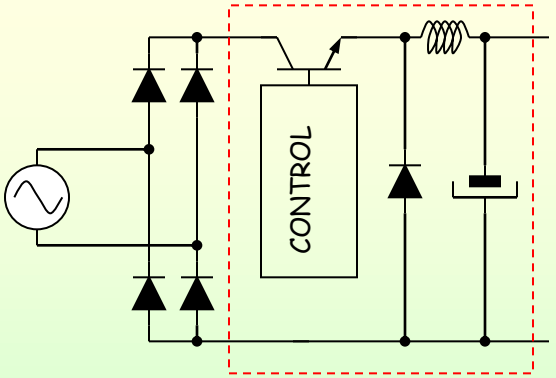


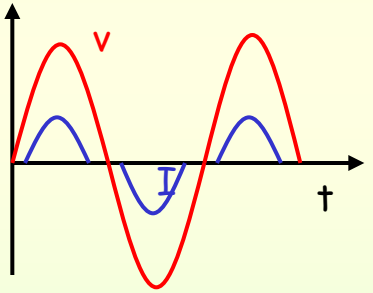


•Con el control adecuado se puede emular el comportamiento de una resistencia.

•Tensiones de bus elevadas (p.e. 400 V)

Reductor (BUCK)
como PFC

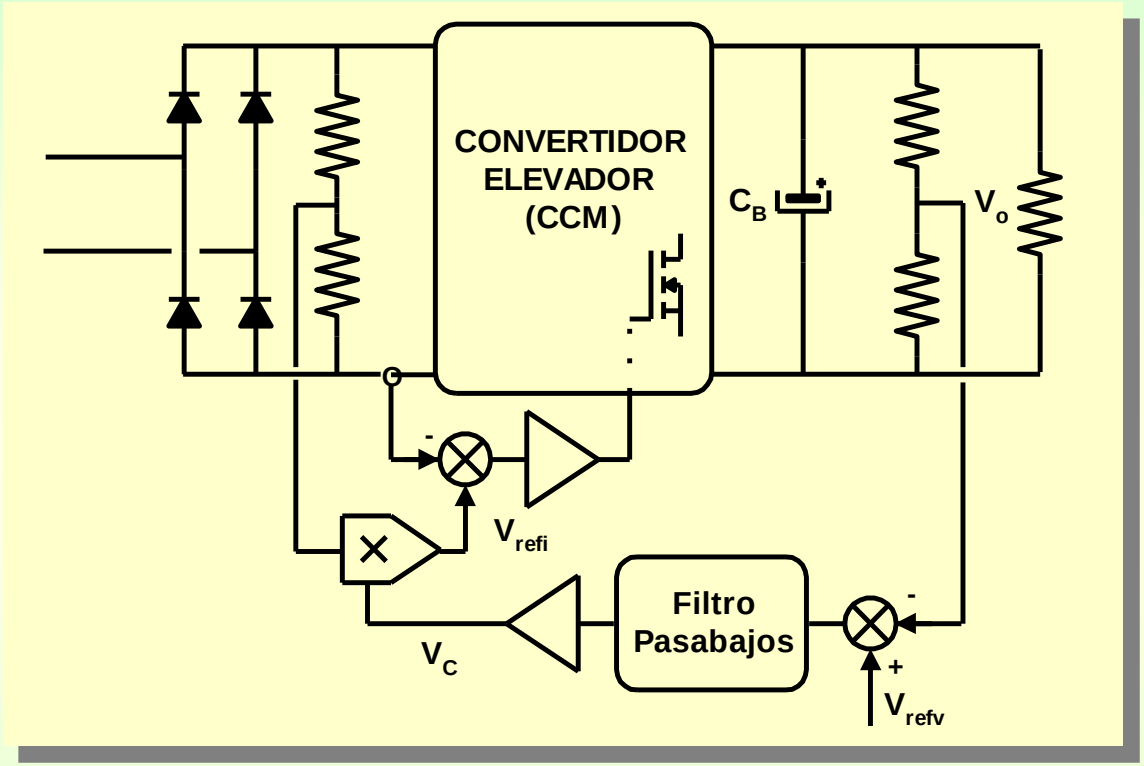




•Siempre existen zonas muertas en la forma de corriente.
•Con ángulos de conducción mayores de 130º se puede cumplir la normativa.

•Tensiones de bus pequeñas (p.e. 120 V)

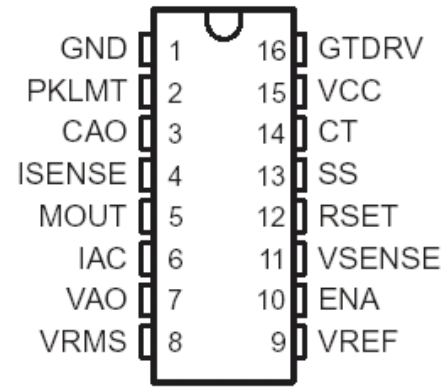
Control de corriente promediado (UC3854).



- Doble lazo de regulación: tensión y corriente.
- INCONVENIENTES:
  - Multiplicador analógico.
  - Lazo de tensión lento.

UC1854B
UC2854A, UC2854B
UC3854A, UC3854B

ADVANCED HIGH-POWER FACTOR PREREGULATOR



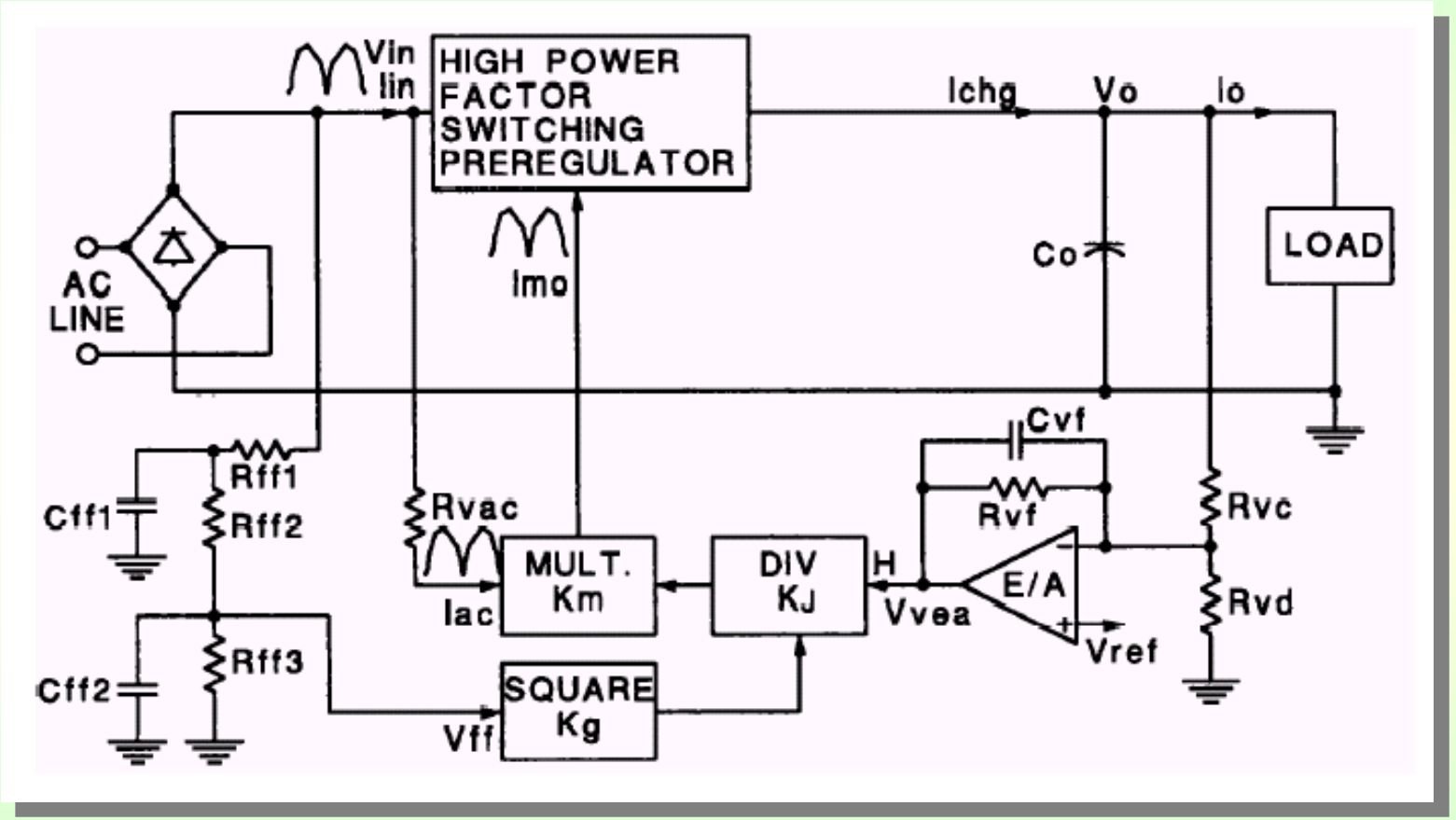
DESCRIPTION

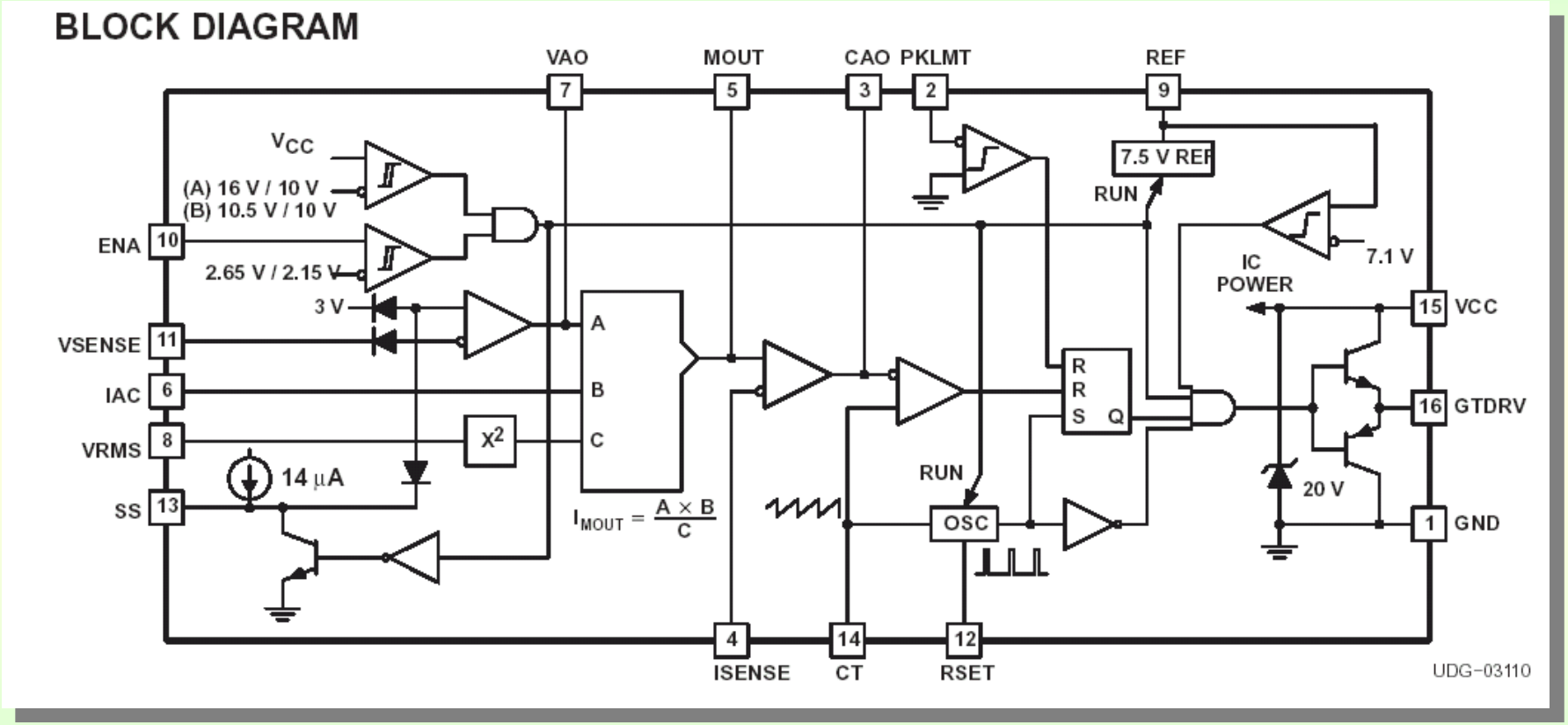
The UC3854A/B products are pin compatible enhanced versions of the UC3854. Like the UC3854, these products provide all of the functions necessary for active power factor corrected preregulators. The controller achieves near unity power factor by shaping the AC input line current waveform to correspond to the AC input line voltage. To do this the UC3854A/B uses average current mode control. Average current mode control maintains stable, low distortion sinusoidal line current without the need for slope compensation, unlike peak current mode control.

A 1% 7.5 V reference, fixed frequency oscillator, PWM, voltage amplifier with soft-start, line voltage feedforward (V_{RMS} squarer), input supply voltage clamp, and over current comparator round out the list of features.

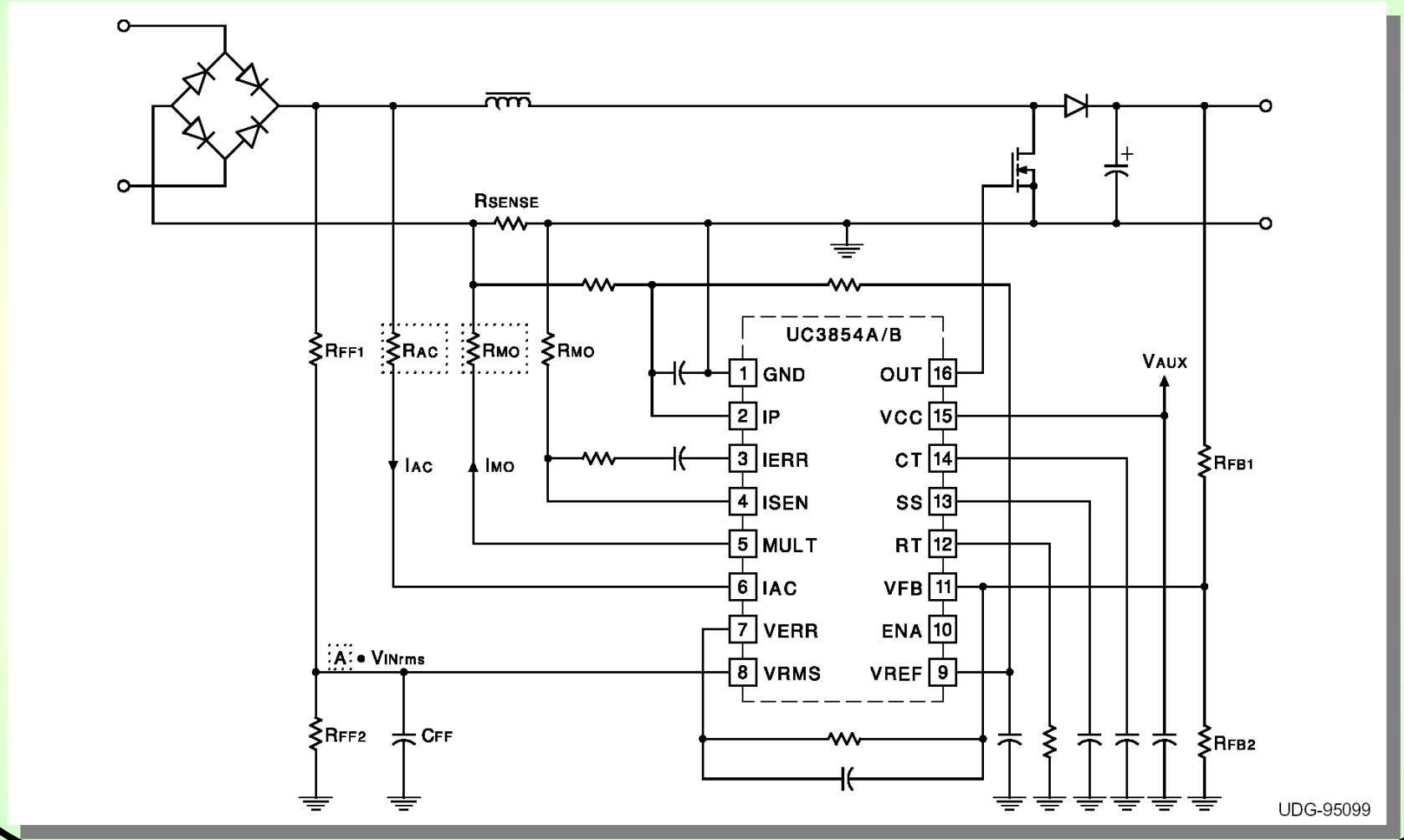
Available in the 16-pin N (PDIP), DW (SOIC-Wide), and J (CDIP) and 20-pin Q (PLCC) package. See ordering information on page 3 for availability by temperature range.

Diagrama funcional de conexionado

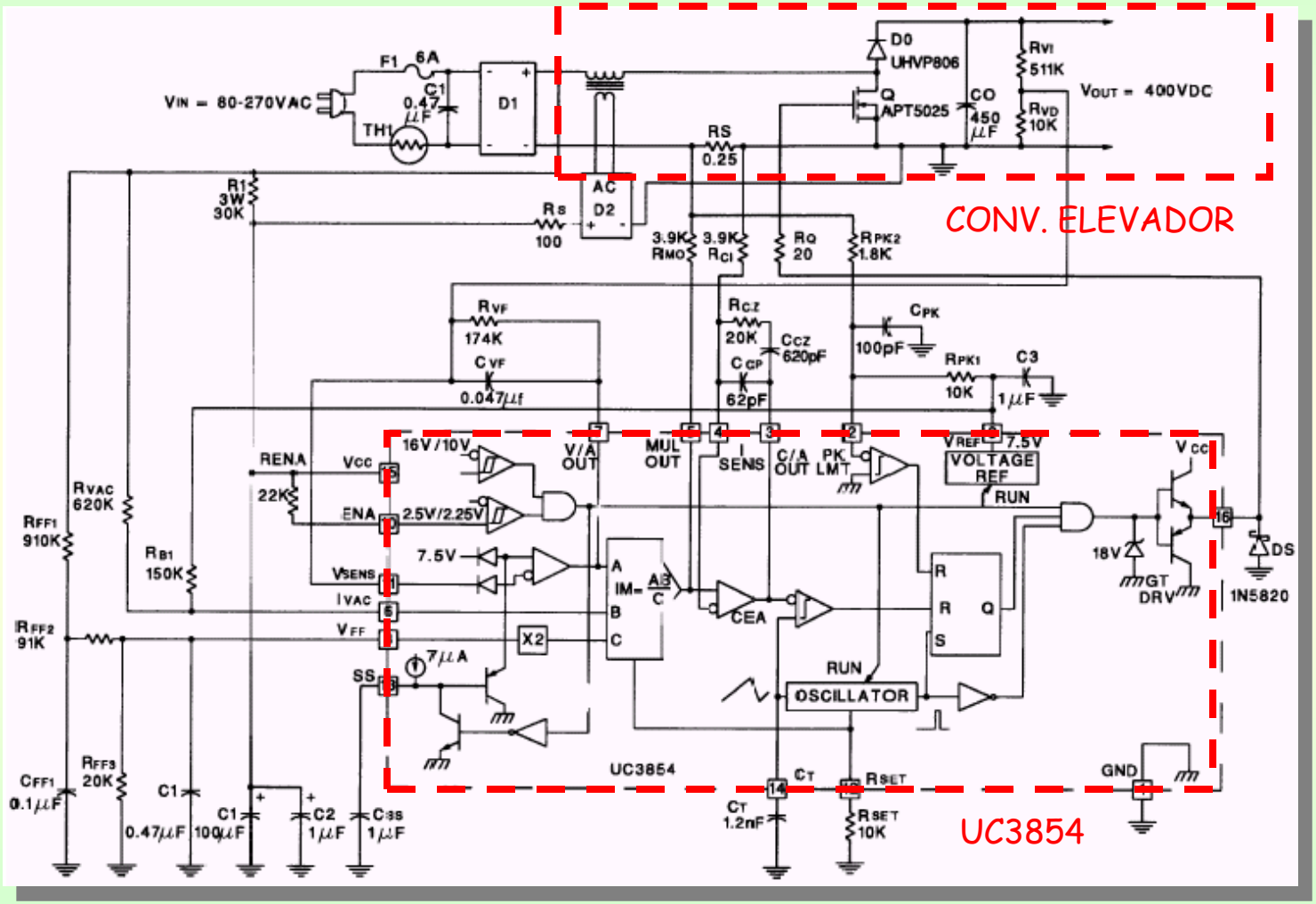



BLOCK DIAGRAM
VAO
MOUT
CAO
PKLMT
REF
7
5
3
2
9
VCC
(A) 16 V / 10 V
(B) 10.5 V / 10 V
ENA
10
2.65 V / 2.15 V
3 V
VSENSE
11
IAC
6
VRMS
8
SS
13
14 µA
X2
A
B
C
IMOUT = A × B / C
7.5 V REF
RUN
IC POWER
7.1 V
15
VCC
16
GTDRV
1
GND
20 V
R
R
S
Q
RUN
OSC
4
14
12
ISENSE
CT
RSET
UDG-03110

Implementación.

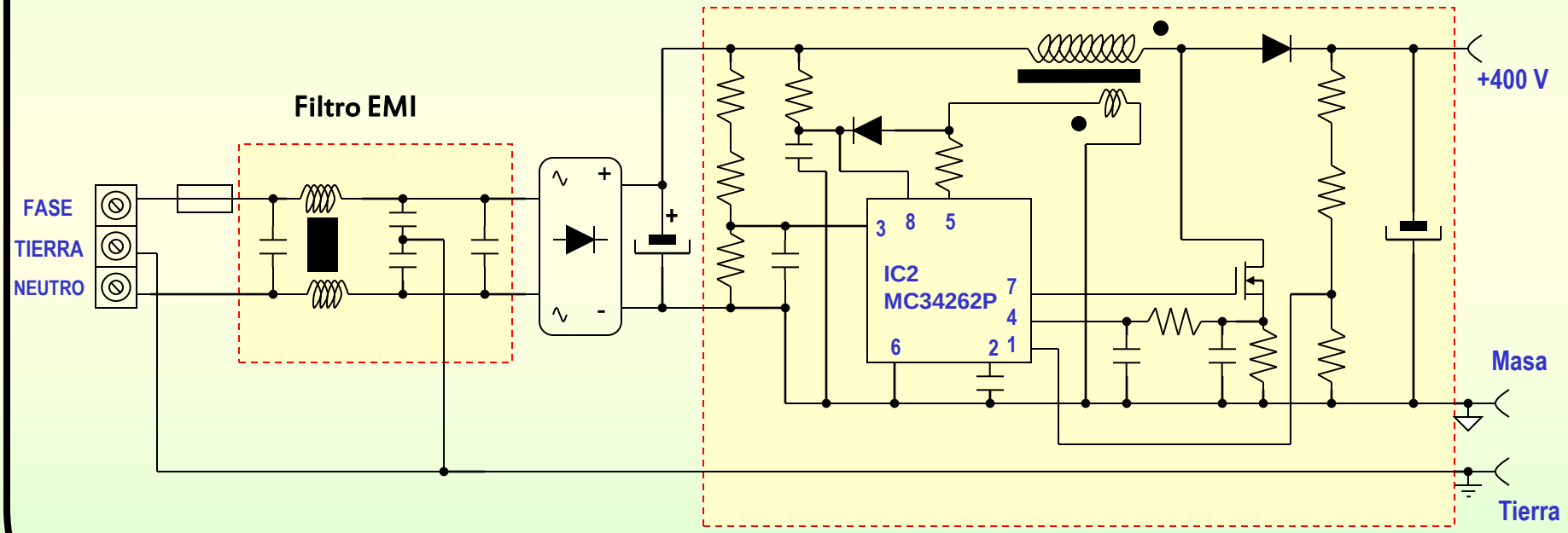


Ejemplo 400V-250W



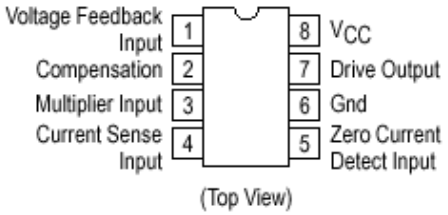
Integrado especializado MC 34262 P

Corrector PFC
Boost trabajando en la frontera CCM/DCM



MC34262
MC33262

PIN CONNECTIONS



(Top View)

MOTOROLA

Power Factor Controllers

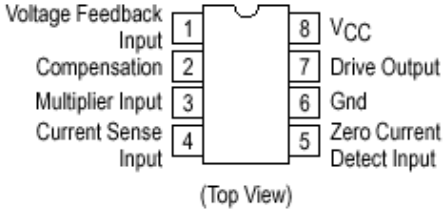
The MC34262/MC33262 are active power factor controllers specifically designed for use as a preconverter in electronic ballast and in off–line power converter applications. These integrated circuits feature an internal startup timer for stand–alone applications, a one quadrant multiplier for near unity power factor, zero current detector to ensure critical conduction operation, transconductance error amplifier, quickstart circuit for enhanced startup, trimmed internal bandgap reference, current sensing comparator, and a totem pole output ideally suited for driving a power MOSFET.

Also included are protective features consisting of an overvoltage comparator to eliminate runaway output voltage due to load removal, input undervoltage lockout with hysteresis, cycle–by–cycle current limiting, multiplier output clamp that limits maximum peak switch current, an RS latch for single pulse metering, and a drive output high state clamp for MOSFET gate protection. These devices are available in dual–in–line and surface mount plastic packages.

- Overvoltage Comparator Eliminates Runaway Output Voltage
- Internal Startup Timer
- One Quadrant Multiplier
- Zero Current Detector
- Trimmed 2% Internal Bandgap Reference
- Totem Pole Output with High State Clamp
- Undervoltage Lockout with 6.0 V of Hysteresis
- Low Startup and Operating Current
- Supersedes Functionality of SG3561 and TDA4817

MC34262
MC33262

PIN CONNECTIONS



(Top View)

Device	Operating Temperature Range	Package
MC34262D	T_A = 0° to +85°C	SO–8
MC34262P		Plastic DIP
MC33262D	T_A = –40° to +105°C	SO–8
MC33262P		Plastic DIP

Simplified Block Diagram

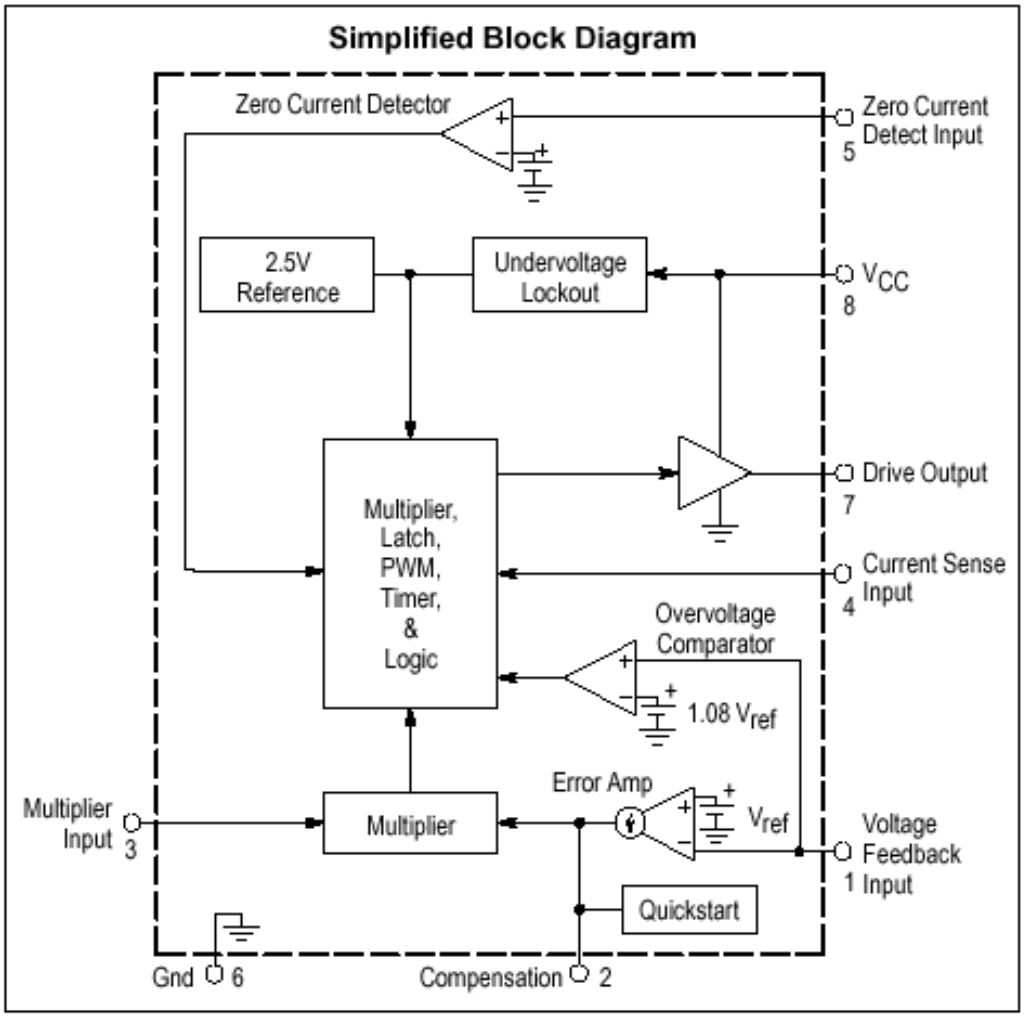


Figure 17. Active Power Factor Correction Preconverter

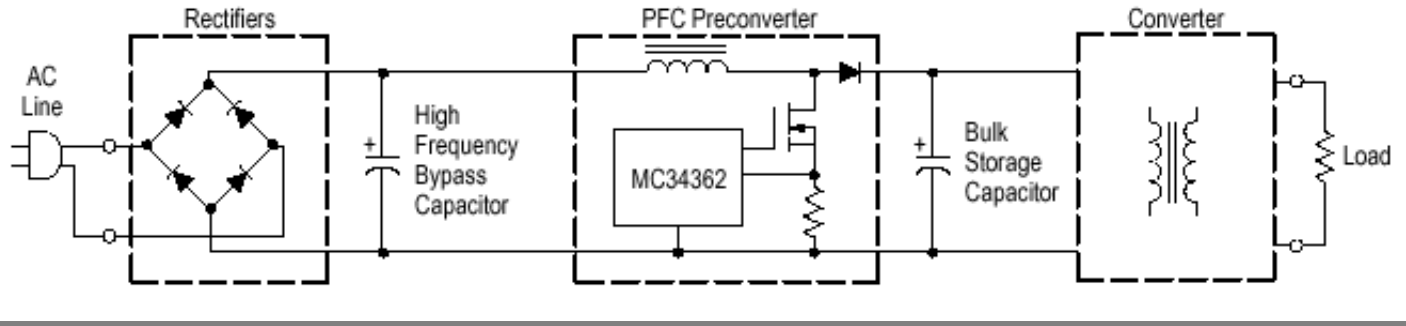
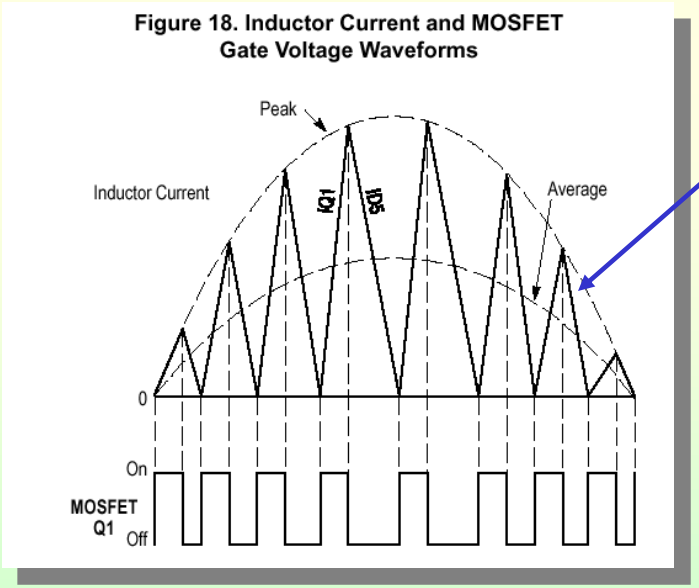


Figure 18. Inductor Current and MOSFET Gate Voltage Waveforms



El convertidor opera en la frontera entre DCM y CCM.

(Esfuerzos de corriente elevados).

El valor medio es siempre proporcional a la tensión de entrada.

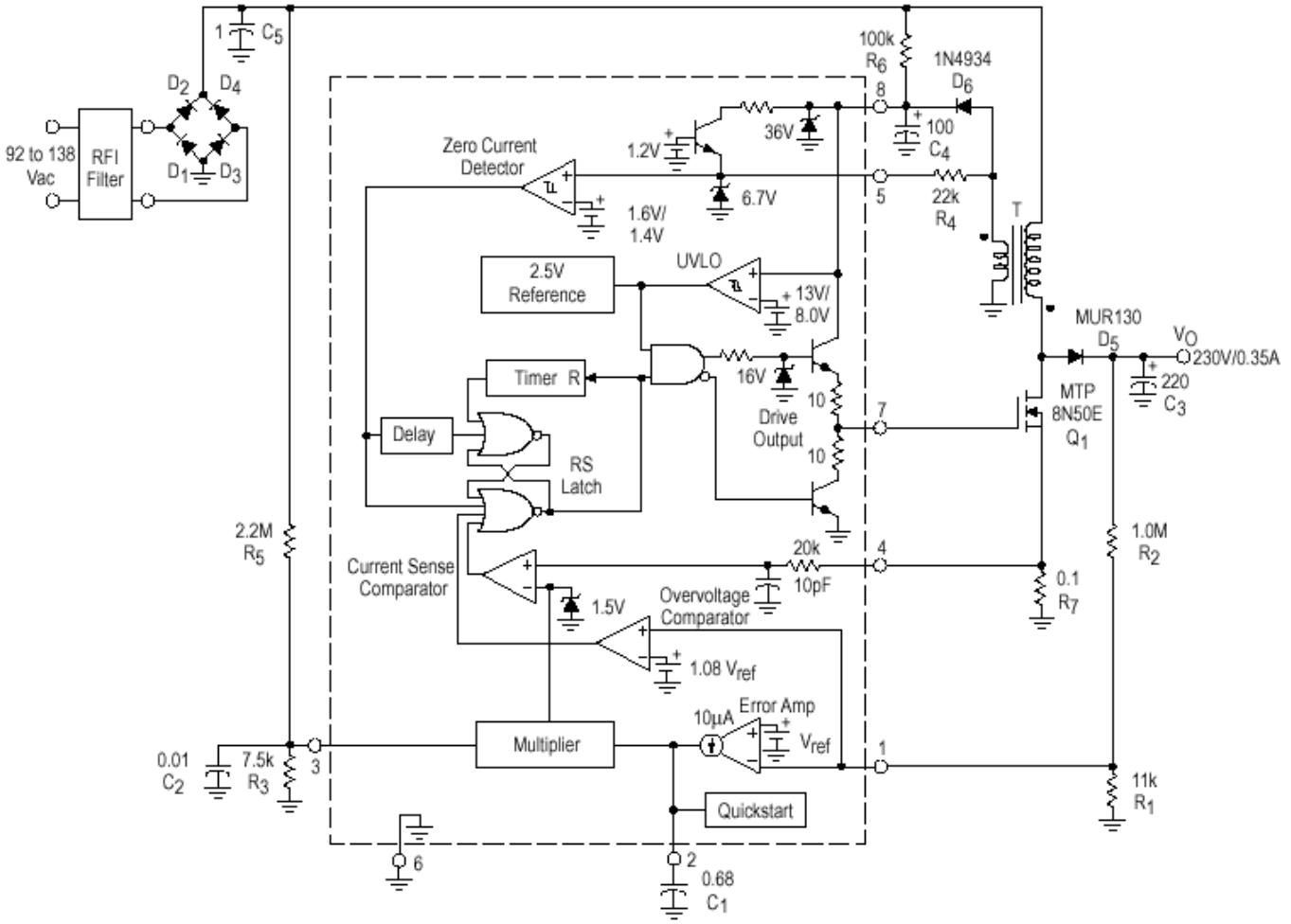
(Emulador de resistencia).

t_{ON}=cte.

Frecuencia de conmutación variable.

Ejemplo de aplicación

Figure 19. 80 W Power Factor Controller



Pasos de diseño

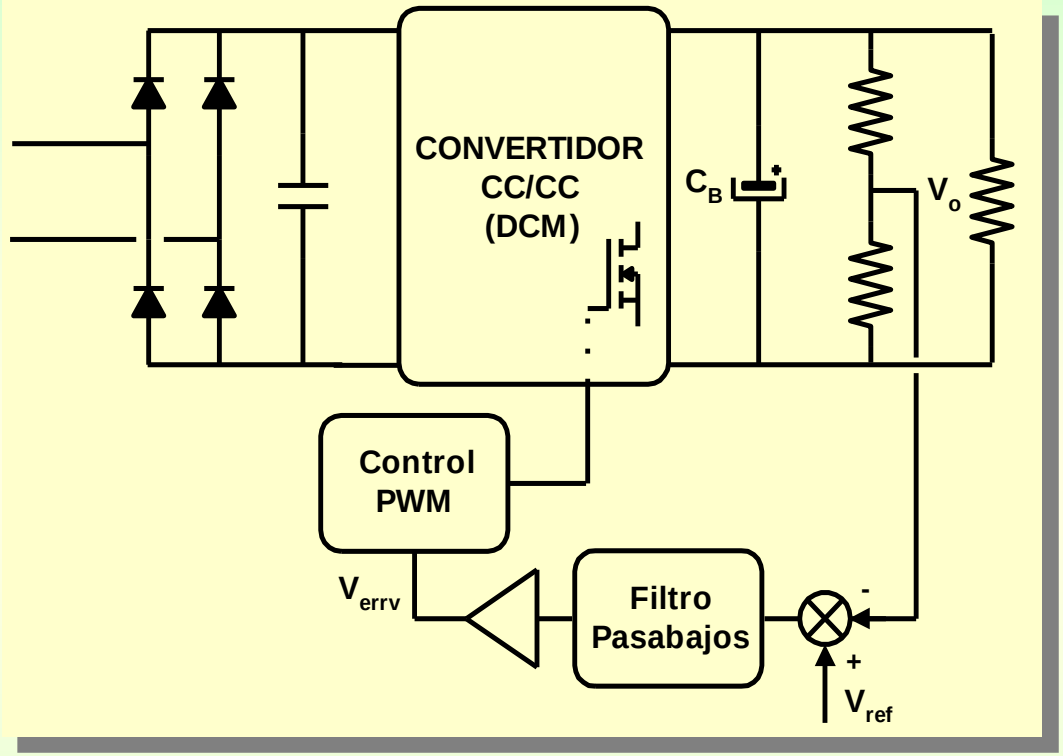
Table 1. Design Equations

Notes	Calculation	Formula
Calculate the maximum required output power.	Required Converter Output Power	$P_O = V_O I_O$
Calculated at the minimum required ac line voltage for output regulation. Let the efficiency $\eta = 0.92$ for low line operation.	Peak Inductor Current	$I_{L(pk)} = \frac{2\sqrt{2}\,P_O}{\eta Vac_{(LL)}}$
Let the switching cycle t = 40 μs for universal input (85 to 265 Vac) operation and 20 μs for fixed input (92 to 138 Vac, or 184 to 276 Vac) operation.	Inductance	$L_P = \frac{t\left(\frac{V_O}{\sqrt{2}} - Vac_{(LL)}\right)\eta\, Vac_{(LL)}^2}{\sqrt{2}\,V_O\,P_O}$
In theory the on–time t_{on} is constant. In practice t_{on} tends to increase at the ac line zero crossings due to the charge on capacitor C_5. Let $Vac = Vac_{(LL)}$ for initial t_{on} and t_{off} calculations.	Switch On–Time	$t_{on} = \frac{2\,P_O\,L_P}{\eta\, Vac^2}$
The off–time t_{off} is greatest at the peak of the ac line voltage and approaches zero at the ac line zero crossings. Theta (θ) represents the angle of the ac line voltage.	Switch Off–Time	$t_{off} = \frac{t_{on}}{\frac{V_O}{\sqrt{2}\,Vac\,\lvert\sin\theta\rvert} - 1}$
The minimum switching frequency occurs at the peak of the ac line voltage. As the ac line voltage traverses from peak to zero, t_{off} approaches zero producing an increase in switching frequency.	Switching Frequency	$f = \frac{1}{t_{on} + t_{off}}$
Set the current sense threshold V_{CS} to 1.0 V for universal input (85 Vac to 265 Vac) operation and to 0.5 V for fixed input (92 Vac to 138 Vac, or 184 Vac to 276 Vac) operation. Note that V_{CS} must be <1.4 V.	Peak Switch Current	$R_7 = \frac{V_{CS}}{I_{L(pk)}}$

Pasos de diseño

Set the multiplier input voltage V_M to 3.0 V at high line. Empirically adjust V_M for the lowest distortion over the ac line voltage range while guaranteeing startup at minimum line.	Multiplier Input Voltage	$V_M = \frac{Vac\ \sqrt{2}}{\left(\frac{R_5}{R_3} + 1\right)}$
The $I_{IB}\ R_1$ error term can be minimized with a divider current in excess of 50 μA.	Converter Output Voltage	$V_O = V_{ref}\left(\frac{R_2}{R_1} + 1\right) - I_{IB}\ R_2$
The calculated peak–to–peak ripple must be less than 16% of the average dc output voltage to prevent false tripping of the Overvoltage Comparator. Refer to the Overvoltage Comparator text. ESR is the equivalent series resistance of C_3	Converter Output Peak to Peak Ripple Voltage	$\Delta V_{O(pp)} = I_O \sqrt{\left(\frac{1}{2\pi f_{ac}\ C_3}\right)^2 + ESR^2}$
The bandwidth is typically set to 20 Hz. When operating at high ac line, the value of C_1 may need to be increased. (See Figure 25)	Error Amplifier Bandwidth	$BW = \frac{gm}{2\ \pi\ C_1}$

Control como seguidor de tensión.



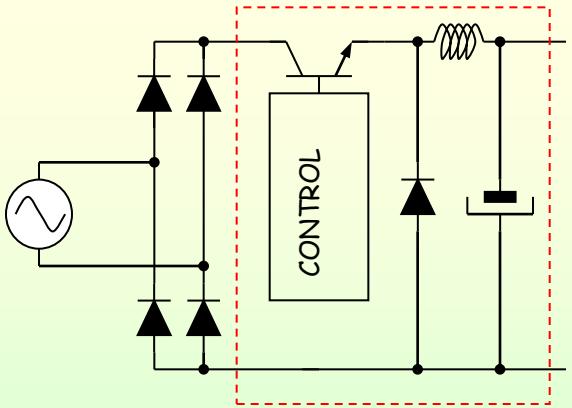
- Funcionamiento:DCM.
- f_C =cte.
- D=cte.

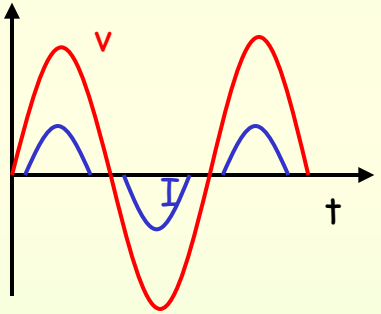
- Lazo de regulación UNICO: tensión.
- VENTAJA: - Simplicidad.
- INCONVENIENTES: - Elevados esfuerzos de corriente, (DCM)
  - Lazo de tensión lento.

Convertidores válidos operando en DCM:

- Flyback. Corriente de entrada senoidal).
- SEPIC. (Corriente de entrada senoidal).
- Reductor (BUCK). (Corriente de entrada NO senoidal).

Reductor (BUCK) como PFC:





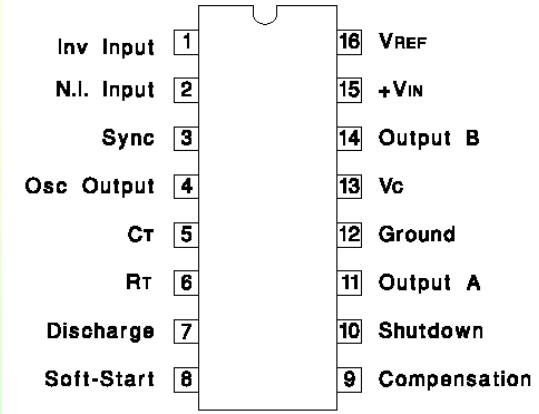
- Siempre existen zonas muertas en la forma de corriente.
- Con ángulos de conducción mayores de 130º se puede cumplir la normativa.
- Tensiones de bus pequeñas (p.e. 120 V)

El integrado puede ser uno estándar PWM: p.e. UC3525

INTEGRATED CIRCUITS
UNITRODE

UC1525A/27A
UC2525A/27A
UC3525A/27A

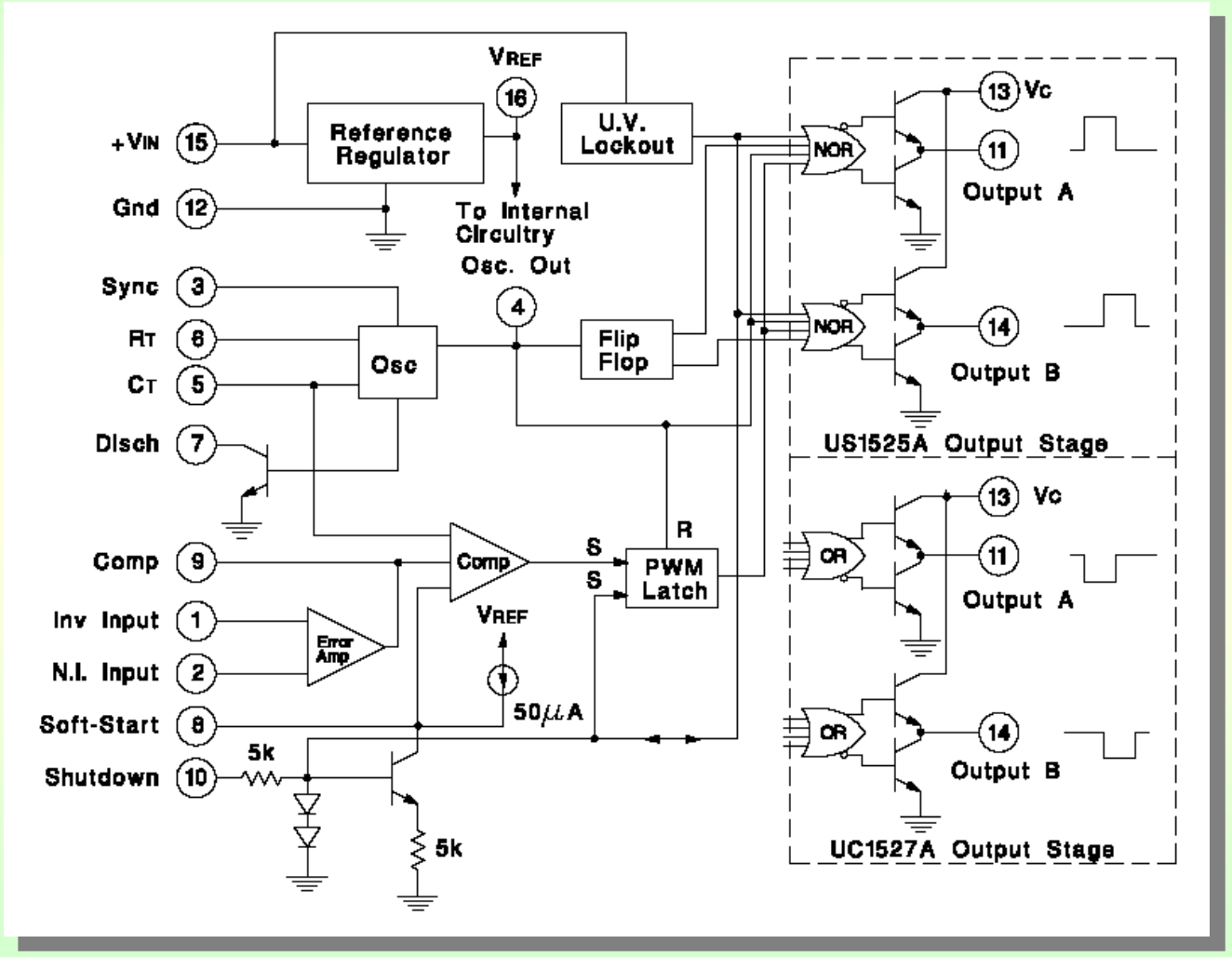
DIL-16 (TOP VIEW)
J or N Package



Regulating Pulse Width Modulators

The UC1525A/1527A series of pulse width modulator integrated circuits are designed to offer improved performance and lowered external parts count when used in designing all types of switching power supplies. The on-chip +5.1V reference is trimmed to ±1% and the input common-mode range of the error amplifier includes the reference voltage, eliminating external resistors. A sync input to the oscillator allows multiple units to be slaved or a single unit to be synchronized to an external system clock. A single resistor between the CT and the discharge terminals provides a wide range of dead-time adjustment. These devices also feature built-in soft-start circuitry with only an external timing capacitor required. A shutdown terminal controls both the soft-start circuitry and the output stages, providing instantaneous turn off through the PWM latch with pulsed shutdown, as well as soft-start recycle with longer shutdown commands. These functions are also controlled by an undervoltage lockout which keeps the outputs off and the soft-start capacitor discharged for sub-normal input voltages. This lockout circuitry includes approximately 500mV of hysteresis for jitter-free operation. Another feature of these PWM circuits is a latch following the comparator. Once a PWM pulse has been terminated for any reason, the outputs will remain off for the duration of the period. The latch is reset with each clock pulse. The output stages are totem-pole designs capable of sourcing or sinking in excess of 200mA. The UC1525A output stage features NOR logic, giving a LOW output for an OFF state. The UC1527A utilizes OR logic which results in a HIGH output level when OFF.

Diagrama de bloques

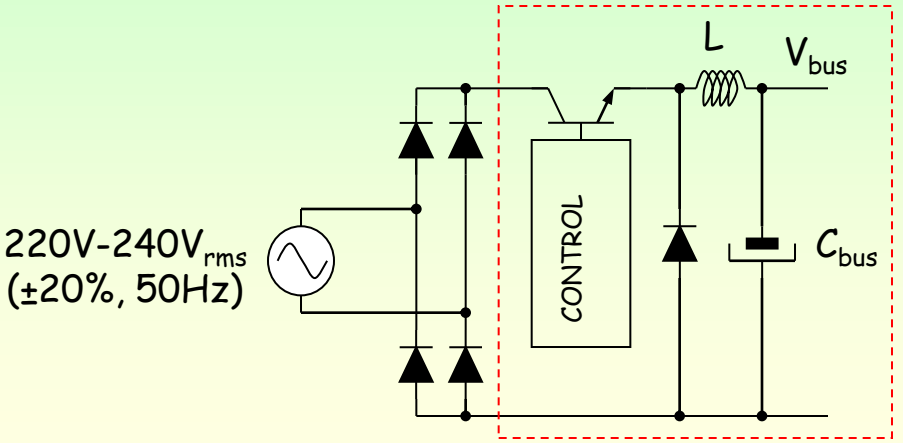


Ejemplo de diseño

Etapa de potencia:

Especificaciones:

- ✓ Tensión europea, Ve: (220V-240V_{rms}, ±20%, 50Hz).
- ✓ V_{bus}.
- ✓ P_{busmax}.
- ✓ Funcionamiento en DCM (PFC).
- ✓ Frecuencia de conmutación (f_C).



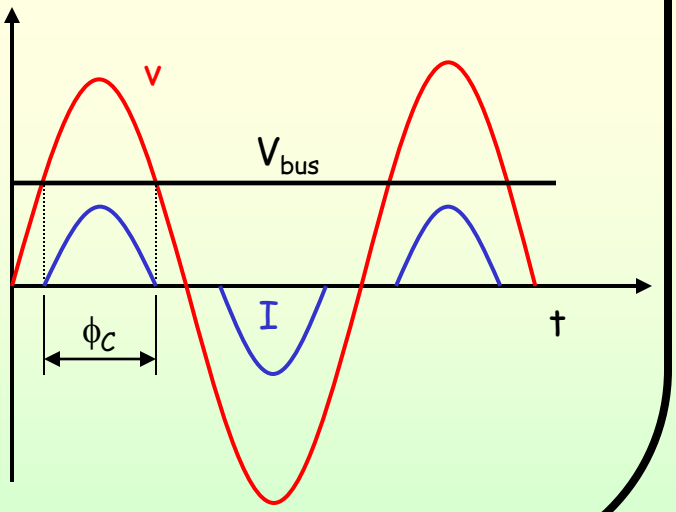
El prerregulador corrector del factor de potencia se diseñará para operar SIEMPRE en DCM a lo largo del ciclo de red.

Se diseñará en las condiciones más desfavorables para el funcionamiento en DCM:

$$V_{emin} = 0{,}8*220V = 176V_{rms}$$

$$\eta_2 = 80\%$$

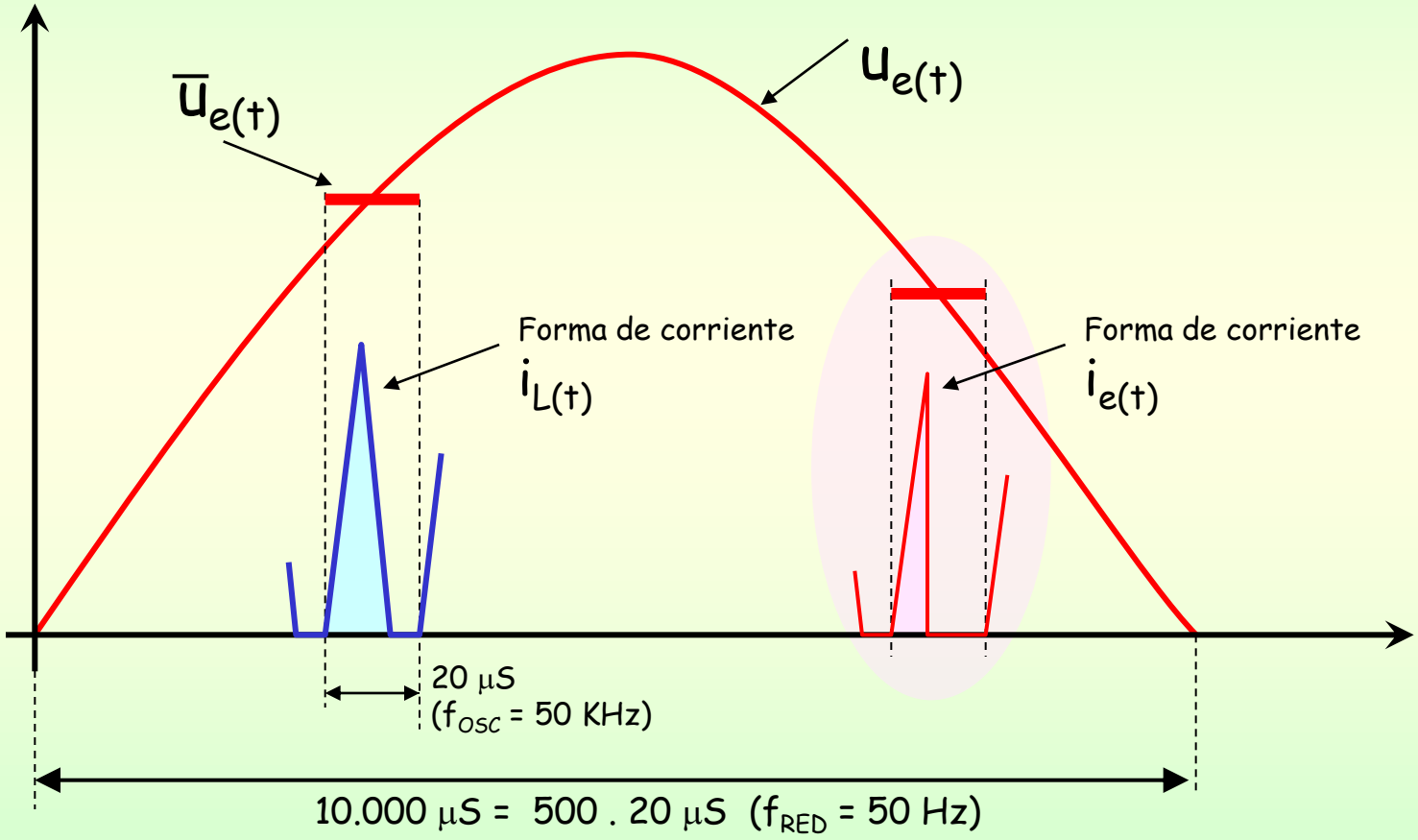
$$P_{busmax} = (1{,}1*P_{LA})/\ \eta_2$$



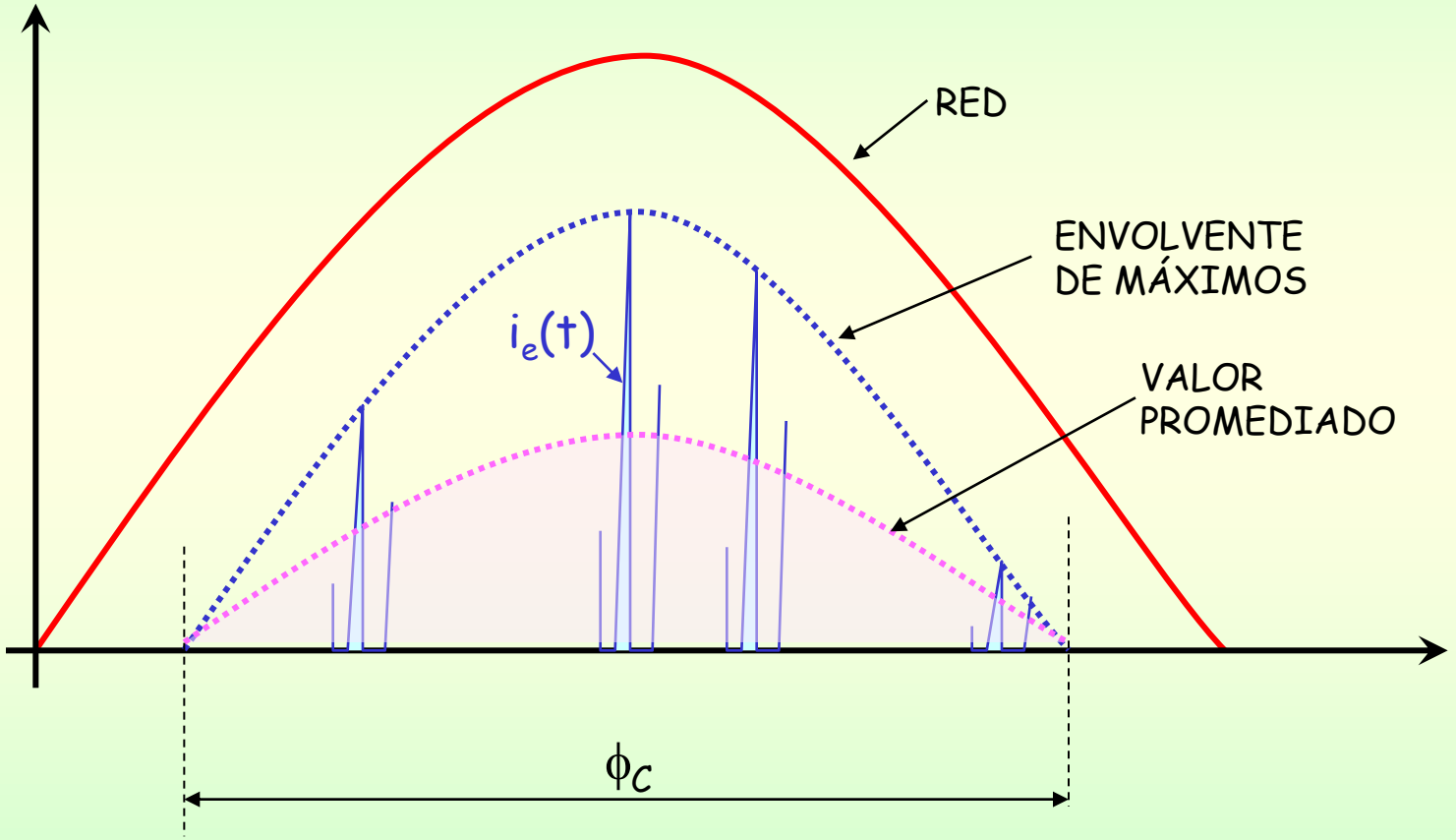
HIPÓTESIS:

Tensión de entrada constante para de cada ciclo de conmutación.

Razonable si $f_{OSC} >> f_{RED}$



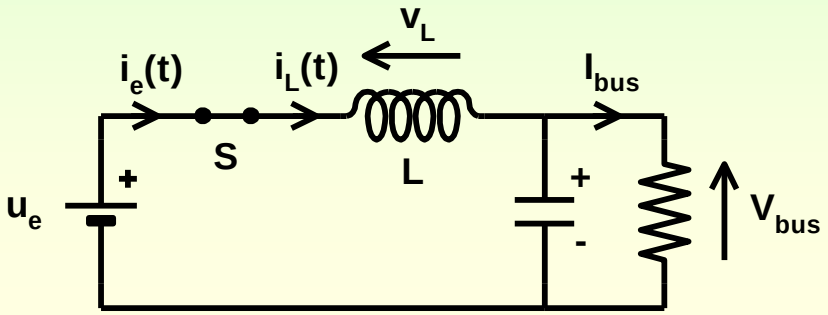
FORMAS DE ONDA DE LA CORRIENTE DE ENTRADA: Operación en DCM



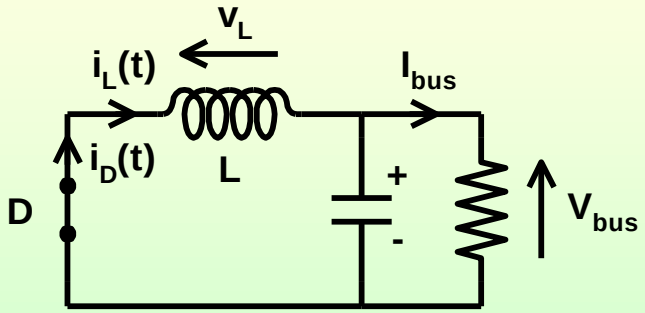
Ejemplo de diseño

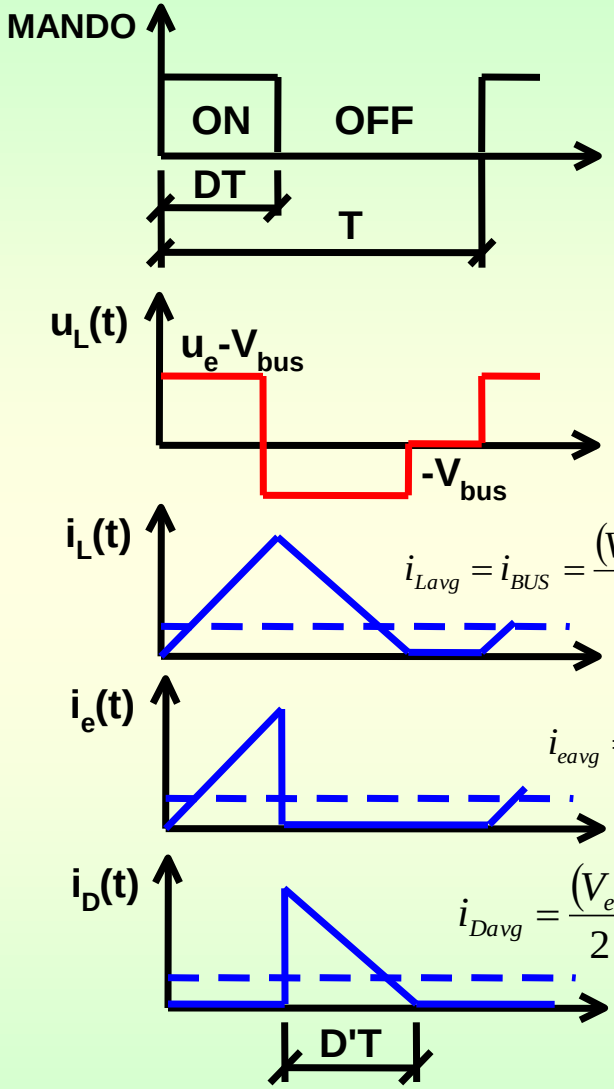
Funcionamiento en DCM a alta frecuencia:

Interruptor cerrado (ON):



Interruptor abierto (OFF):





Ejemplo de diseño

Como la tensión de entrada es senoidal, las formas de onda de las corrientes medias, evolucionarán en el tiempo:

$$\frac{\pi-\phi_C}{2} \le \omega t \le \frac{\pi+\phi_C}{2}$$

Entrada:

$$i_{eavg}(\omega t) = \frac{\left(\sqrt{2}\cdot V_e \cdot sen\,\omega t - Vbus\right)\cdot D^2}{2\cdot L\cdot f_C}$$

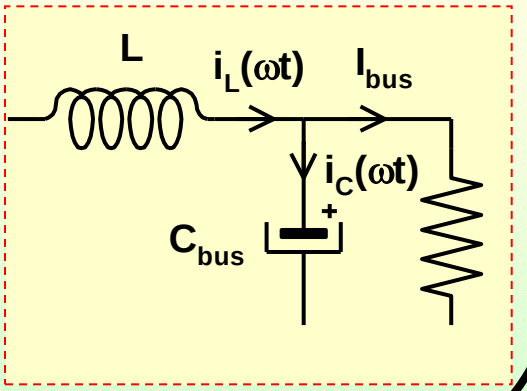
Bobina:

$$i_{Lavg}(\omega t) = \frac{\sqrt{2}\cdot V_e \cdot sen\,\omega t \cdot D^2}{2\cdot L\cdot f_C}\cdot\left(\frac{\sqrt{2}\cdot V_e \cdot sen\,\omega t}{V_{bus}} - 1\right)$$

Condensador:

$$i_{Cavg}(\omega t) = i_{Lavg} - I_{bus}$$

$$i_{Cavg}(\omega t) = \frac{\sqrt{2}\cdot V_e \cdot sen\,\omega t \cdot D^2}{2\cdot L\cdot f_C}\cdot\left(\frac{\sqrt{2}\cdot V_e \cdot sen\,\omega t}{V_{bus}} - 1\right) - \frac{P_{bus}}{V_{bus}}$$



Ejemplo de diseño

La potencia entregada a la salida será:

$$P_{bus} = \frac{1}{\pi} \cdot \int_0^{\pi} i_{eavg}(\omega t) \cdot v_e(\omega t) \cdot d(\omega t) = \frac{1}{\pi} \cdot \int_{\frac{\pi-\varphi_C}{2}}^{\frac{\pi+\varphi_C}{2}} i_{eavg}(\omega t) \cdot v_e(\omega t) \cdot d(\omega t)$$

operando:

$$P_{bus} = \frac{D^2 \cdot V_e^2 \cdot (\phi_C - sen\phi_C)}{2 \cdot L \cdot \pi \cdot f_C}$$

¿f_C, D y L?

Ángulo de conducción, ϕ_C:

$$\sqrt{2} \cdot V_e \cdot sen\left(\frac{\pi - \phi_C}{2}\right) = V_{bus} \Rightarrow \phi_C = \pi - 2 \cdot arcsen\frac{V_{bus}}{\sqrt{2} \cdot V_e}$$

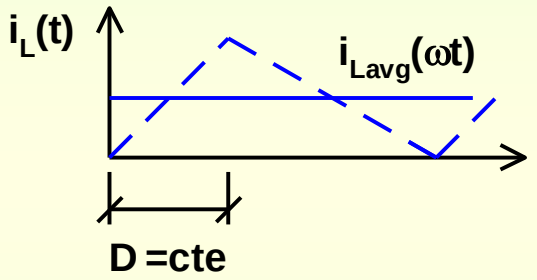
(en radianes).

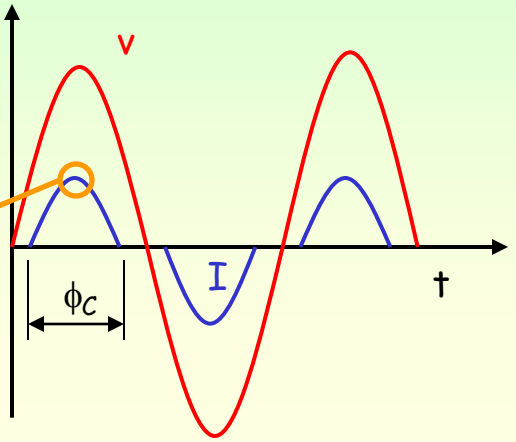
Ejemplo de diseño

Ciclo de trabajo, D:

Interesa que los esfuerzos de corriente sean lo mínimos posible y que siempre funcione en DCM y D=Cte.

En el momento de cresta debe estar en frontera DCM-CCM:





Al operar en CCM:

$$D_{MAX} = D_{CCM} = \frac{V_{bus}}{\sqrt{2} \cdot V_{eMIN}}$$

Con lo que se puede obtener la L necesaria para entregar una determinada potencia y para el D_{MAX}:

$$L = \frac{V_{bus}^2 \cdot (\phi_C - sen\,\phi_C)}{4 \cdot \pi \cdot P_{bus} \cdot f_C}$$

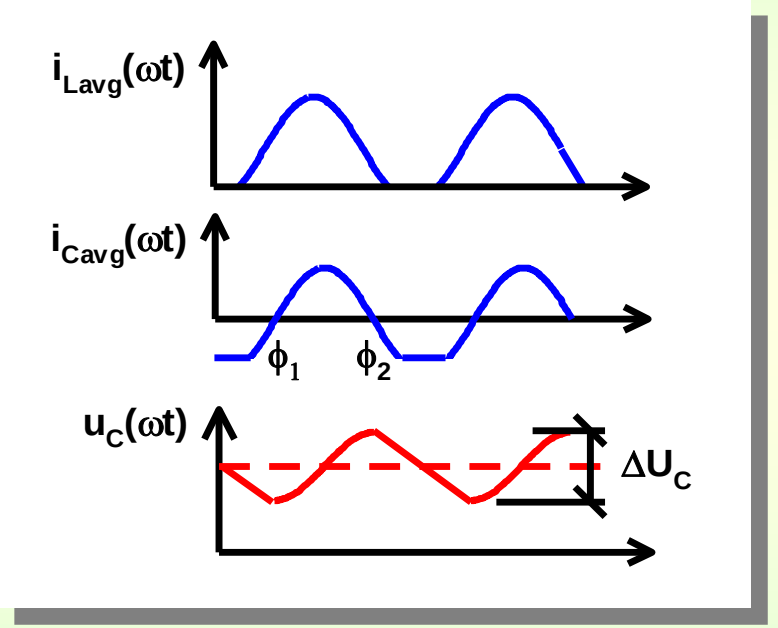
Ejemplo de diseño

El condensador se calcula según unas especificaciones de rizado, DU_C:

$$i_{Cavg}(\omega t) = i_{Lavg}(\omega t) - I_{bus}$$

$$\Delta U_C = \frac{1}{C_{bus}} \cdot \int_{\phi_1}^{\phi_2} i_{Cavg}(\omega t) \cdot d\,\omega t$$

$$i_{Cavg}(\omega t) = 0 \Rightarrow \phi_1 \; ; \quad \phi_2 = \pi - \phi_1$$



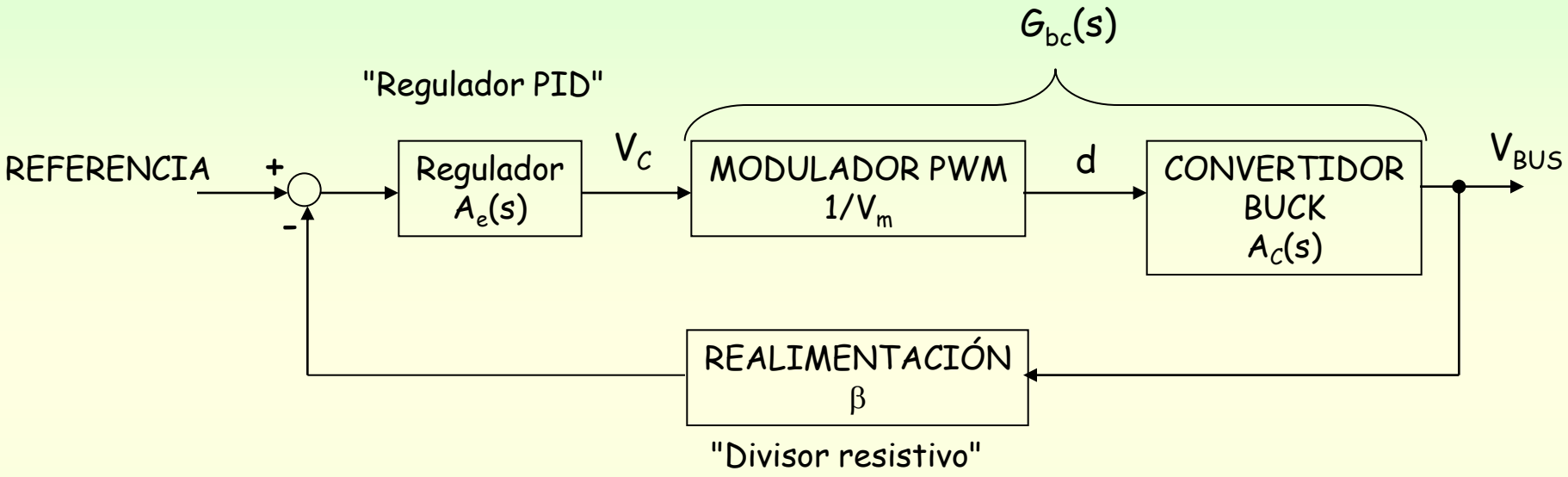
Esfuerzos máximos de tensión en los semiconductores:

Transistor: $V_{ds\max} = \sqrt{2} \cdot V_e$

Diodo: $V_{dinv\max} = \sqrt{2} \cdot V_e$

Ejemplo de diseño

REGULACIÓN:

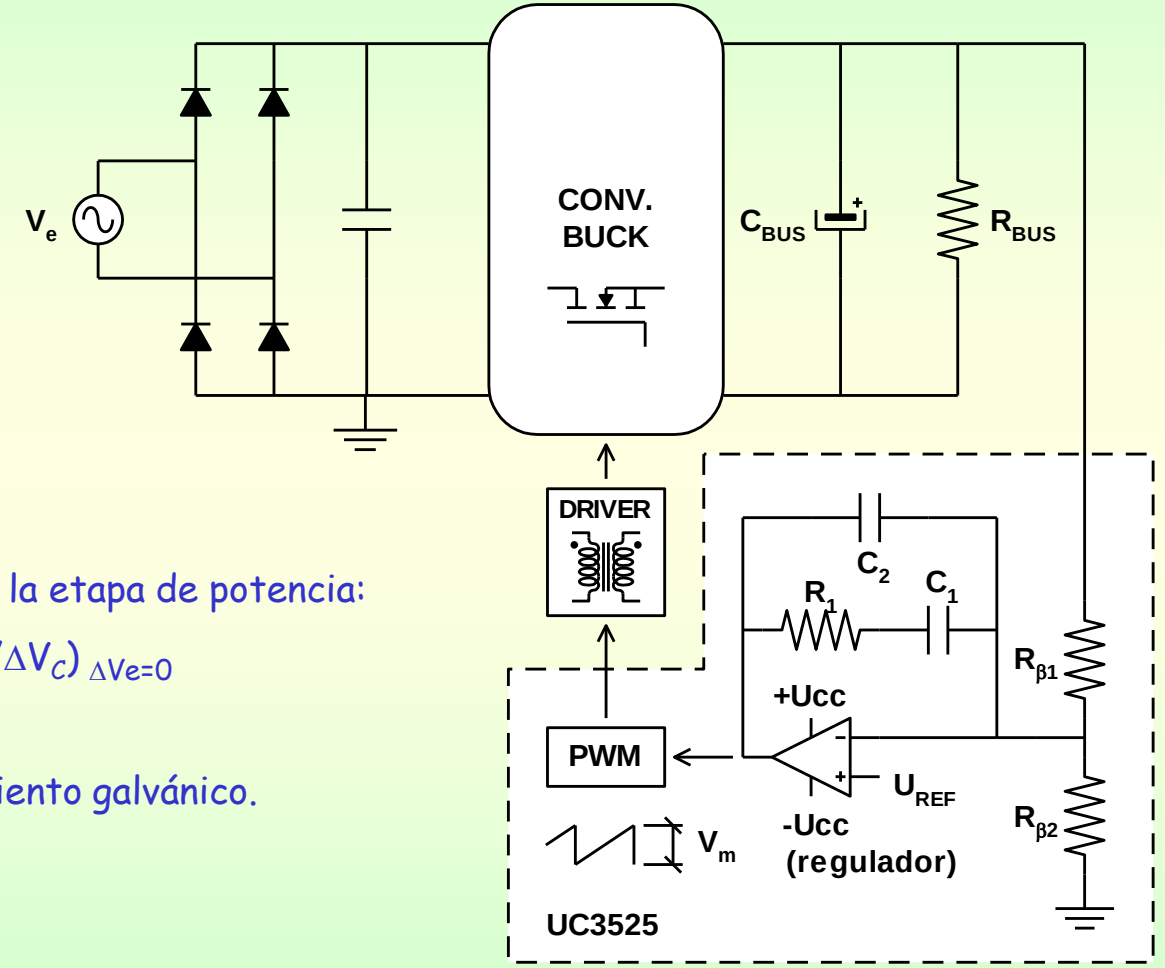


ES NECESARIO REGULAR LA TENSIÓN DE SALIDA.

CUANDO LA POTENCIA DISMINUYE ES NECESARIO DISMINUIR EL CICLO DE TRABAJO (d) PARA ESTABILIZAR LA TENSIÓN DEL BUS

Ejemplo de diseño

Etapa de control:



- Función de transferencia de la etapa de potencia:

$$G_{bc}(s)=(\Delta V_{bus}/\Delta V_C)_{\Delta Ve=0}$$

- Diseño del regulador.
- Diseño del driver con aislamiento galvánico.

Ejemplo de diseño

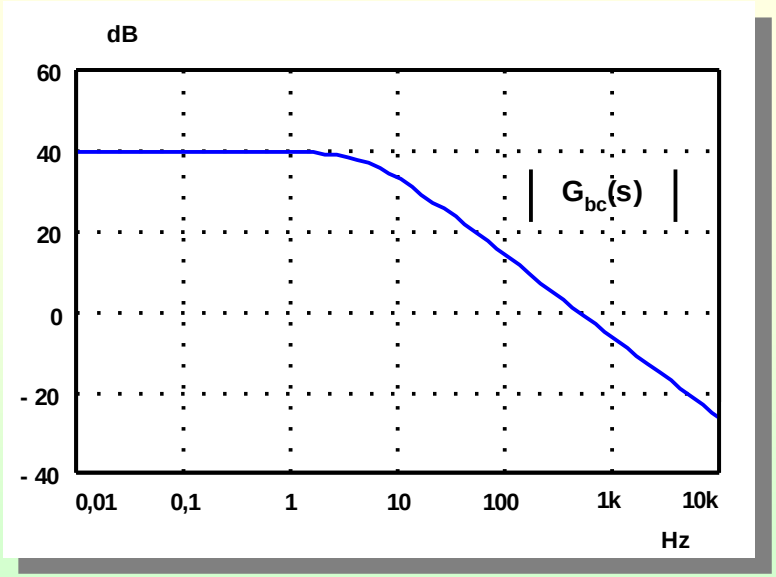
Función de transferencia de la etapa de potencia: $G_{bc}(s)=(\Delta V_{bus}/\Delta V_C)_{\Delta Ve=0}$

$$G_{bc}(s) = g_c \cdot \frac{(r_o \,//\, R_{bus})}{1 + s \cdot C_{bus} \cdot (r_o \,//\, R_{bus})}$$

donde:

$$g_C = \frac{V_e^2 \cdot T_s \cdot D}{L \cdot \pi \cdot V_{bus} \cdot V_m} \cdot (\phi_c - sen(\phi_c)) \qquad \frac{1}{r_o} = \frac{P_{bus}}{V_{bus}^2} + \frac{V_e^2 \cdot T_s \cdot D^2}{L \cdot \pi \cdot V_{bus}} \cdot \frac{1}{\sqrt{2 \cdot V_e^2 - V_{bus}^2}}$$

Ejemplo:

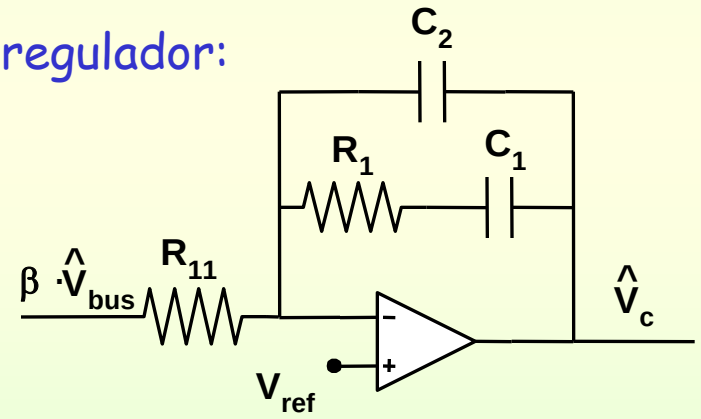


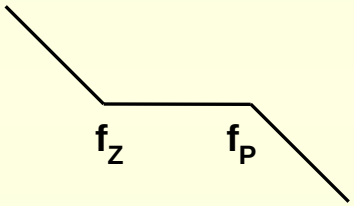
Ejemplo de diseño

Diseño del regulador:

- Estabilidad a lo largo de la vida útil de la lámpara (MF = 45º).
- Reducido ancho de banda, (10-20Hz).
- Error de posición nulo (acción integral).

Topología del regulador:





Función de transferencia:

$$A_e(s) = \frac{1 + SR_1C_1}{SR_{11}(C_1 + C_2)\left(1 + SR_1\left(\frac{C_1C_2}{C_1 + C_2}\right)\right)}$$

$$R_{11} = R_{\beta 1} // R_{\beta 2}$$

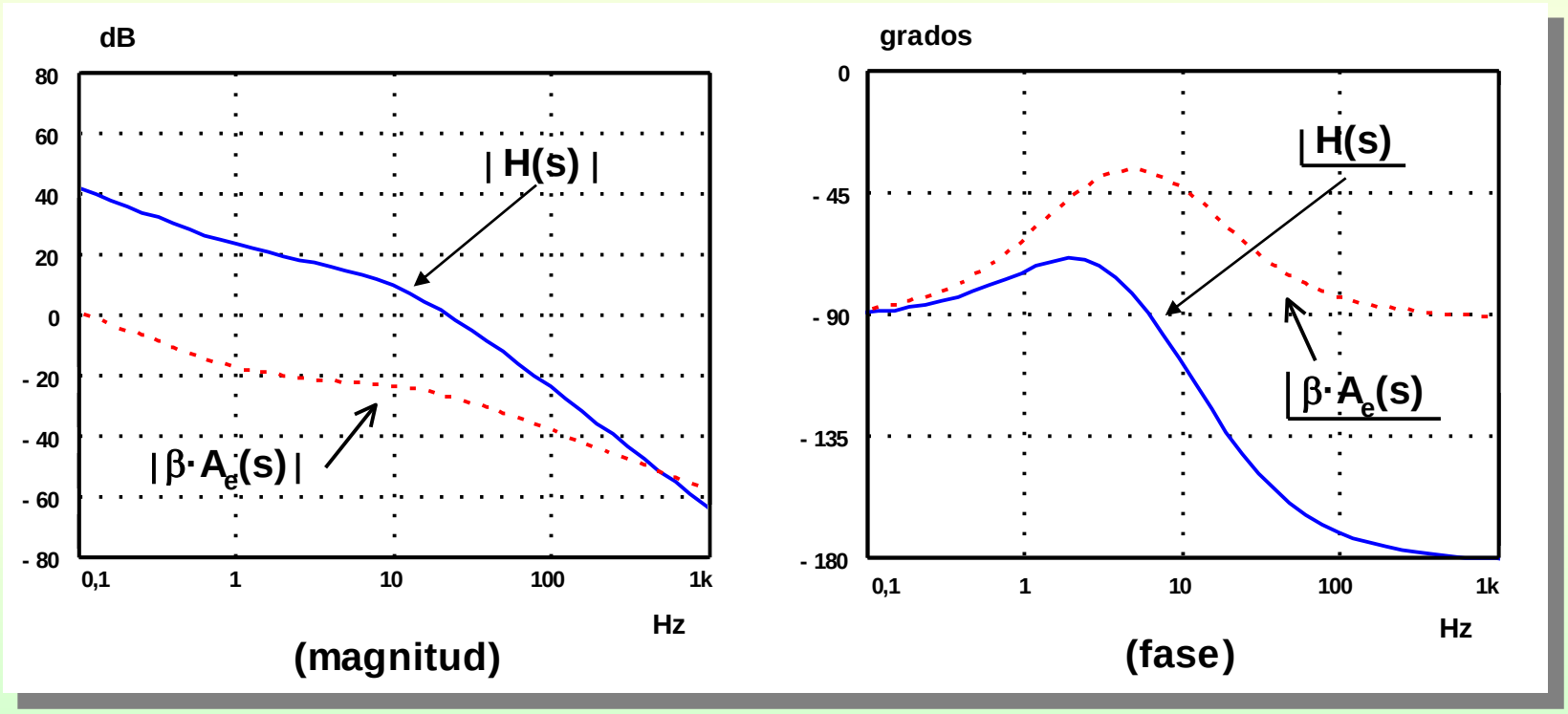
$$f_Z = \frac{1}{2\pi R_1C_1}$$

$$f_P = \frac{1}{2\pi\ R_1\left(\frac{C_1C_2}{C_1 + C_2}\right)}$$

Ejemplo de diseño

Diseño del lazo de realimentación:

- La ganancia de lazo, $H(s) = G_{bc}(s)\cdot\beta\cdot A_e(s)$, debe ser la de un integrador pasando por 0 dB con un margen de fase de 45º.



Ejemplo de diseño

Driver con aislamiento: