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Review

Review of DC-DC Partial Power Converter Configurations and Topologies

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Abstract: The Partial Power Processing (PPP) concept has garnered attention as it enables the downsizing of converter and component ratings. Unlike conventional power processing, PPP addresses a portion of the transferred power, leading to a reduction in conversion losses. Throughout this paper, the state of the art of isolated and non-isolated DC-DC converter topologies will be revised. Partial Power Converter (PPC) systems represent one of the main streams of PPP, which, based on isolation requirements and converter connections, can further be divided into *isolated* converters, such as: Input-Parallel-Output-Series (IPOS), Input-Series-Output-Parallel (ISOP), and, Input-Series-Output-Series (ISOS), or *non-isolated* converters. This work intends to evaluate and differentiate the characteristics of each type of topology while developing analytically possible connections that may require further research and reviewing *metrics* that help in fair comparisons of different PPC arrangements, operating under different conditions. A thorough revision is provided for DC-DC converter topologies due to their increased importance in present-day applications, such as energy storage, Electric Vehicles (EVs), and Photo-Voltaics (PVs).

Keywords: partial power processing (PPP); partial power converter (PPC); input-parallel-output-series (IPOS); input-series-output-parallel (ISOP); input-series-output-series (ISOS); input-parallel-output-parallel (IPOP); fractional power converters (FPC)

Citation: Gsous, O.; Rizk, R.; Barbón, A.; Georgious, R. Review of DC-DC Partial Power Converter Configurations and Topologies. *Energies* **2024**, *17*, 1496. https://doi.org/10.3390/en17061496

Academic Editor: Alon Kuperman

Received: 8 February 2024
Revised: 11 March 2024
Accepted: 18 March 2024
Published: 21 March 2024

1. Introduction

Recent trends in electrical power, such as the rising electrification across sectors and the expanding integration of renewable resources and energy storage applications, have ignited heightened interest in power electronics and power converters [1–3]. The demand in the power electronics field has led to the development of new concepts as well as revisiting concepts that are already in use, which brought the PPP field into existence. One of the major examples of PPP related to renewable energy generation is the Double-Fed Induction Generator (DFIG) [4]. The DFIG was introduced to the wind energy generation field as an advancement to overcome the disadvantages of the Adjustable-Speed Generator (ASG) [5]. The main advantage of DFIG over ASG is that it enables the use of the partial power converter. This leads to a reduction in the total cost of the system due to reducing the size of the inverter as well as the filter's passive components. In PPP, as the name indicates, a power converter is used to process only a part of the whole power, thus reducing the losses and permitting a reduction in components size [6].

The majority of the applications of PPP are based on DC-DC converters due to the nature of the current flow, and the fact that several applications have varying input or output voltage, which is a common situation for PVs and battery applications, while it is not common to encounter the same in AC, where the input and output voltages are usually well defined. Nevertheless, PPC can be integrated into the DC side of DC-AC converters to obtain a PPP feature for AC applications. Furthermore, pure DC-AC topologies also

exist, such as in the work of [7], where they propose handling power conversion by higher rating IGBT master units, and a SiC MOSFET slave unit is coupled by line-frequency transformer to deal with *partial power* voltage regulation and harmonic compensation. Another interesting application for AC-DC appears as an ancillary feature in the work of [8], where PPP is implemented to provide *hold-up* time compensation.

Another application of DC-AC partial power topologies was demonstrated by [9], where the inputs of two DC-DC converters were connected in parallel to the same PV module, and hence a differential-mode sinusoidal output was achieved directly.

This paper will follow the nomenclature suggested by Anzola et al. [4], which segregates PPP into three broad families, as demonstrated in Figure 1. The first group in Figure 1 is the Differential Power Processing (DPP) topology. It deals mainly with current differences in series connected elements; this is also referred to as Parallel Current Regulator (PCR) in the work of Santos, Zientarski, and Martins [2]. The Photo-Voltaic (PV) *optimizer* is one salient example of the Differential Power Converter (DPC). Active battery cell balancing topologies also belong to this category. Such devices deal with the *mis-match* current between elements connected in series [1,4,10]. This is a desirable feature that extends the capability of PV arrays or battery cells, where those systems are usually composed of series-connected sources, with the performance of the whole group limited by the weakest link.

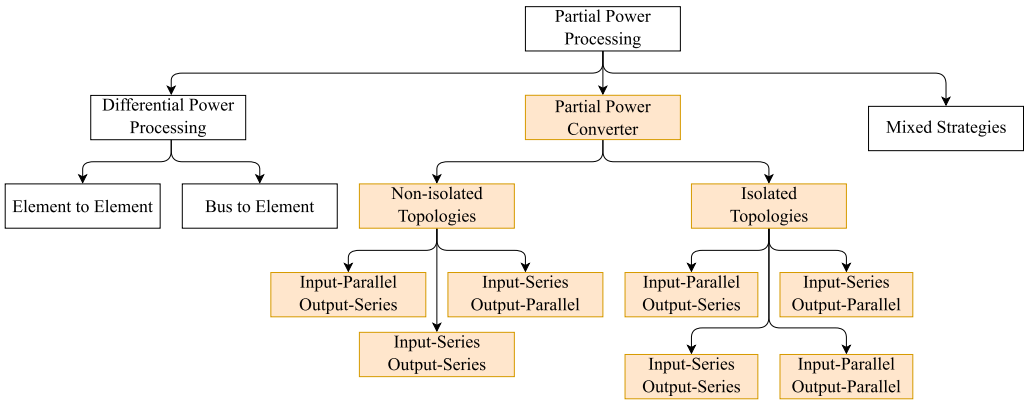

Figure 1. PPP family tree influenced by [4], with the scope of the current work highlighted.

The second branch of the PPP family tree is PPC (referred to as Series Voltage Regulator (SVR) by [2]), which can further be distinguished into two groups based on isolation requirements; however, it is to be noted that whether isolation is required for the converter does not imply the fact that the overall system will not have inherited galvanic isolation between its input and its output. The main advantage of PPC operation is its ability to interface a varying voltage on one side (either *source* or *load*) to a fixed voltage on the other side, which is a valuable feature for Maximum Power Point Tracking (MPPT) systems and battery charging applications [6]. The sub-group of the *isolated* topologies further splits into sub-groups: Input-Series-Output-Parallel (ISOP) (also referred to as Series-Input-Parallel-Output (SIPO) in some studies), Input-Parallel-Output-Series (IPOS) (or Parallel-Input-Series-Output (PISO)), Input-Series-Output-Series (ISOS), and Input-Parallel-Output-Parallel (IPOP). Various possible arrangements are revised in the upcoming Section 3. The sub-group of non-isolated PPP deals solely with the Fractional Power Converter (FPC), and will be revised in Section 4.1.

The last group seen in Figure 1 is the *mixed* strategies, where topology belonging to this group mixes the two previous designs (i.e., the DPC and PPC) in order to obtain the advantages of both groups while avoiding their shortfalls [4].

Section 2 will revise the present-day parameters used to *benchmark* designs and the performance of proposed PPP topologies and comment on the grouping and categorizing of the various PPP families. Section 3 analyzes the fundamental current and voltage relations of the *isolated* PPP and uses the parameters developed in Section 2 to derive theoretical

operating limits. An assorted collection of designs is also reviewed in Section 3.2 (for IPOS), Section 3.4 (for ISOP), and Section 3.6 (for ISOS). Section 4.1 will review possible FPC architectures, and some examples from the literature will be revised in Section 4.2. Finally, Section 5 includes the conclusions of this work.

2. Comparison Metrics

Several aspects and merits are implemented to enable comparison between various topologies. This section will revisit and define such attributes, starting with one of the main features of any power conversion system, *efficiency* (η). Given the fact that the PPC treats only a fraction of the whole transferred power, this will give rise to two different dimensionless parameters [4]: *System efficiency* (η_{sys}), which is defined as the ratio of *load power* (P_{Load}) to the *source power* (P_{source}), and further in terms of Source/Load currents (I_{Source}, I_{Load}), and Source/Load voltages (V_{Source}, V_{Load}), as stated in (1) [11–13].

$$\eta_{sys} = \frac{P_{Load}}{P_{Source}} = \frac{V_{Load} \cdot I_{Load}}{V_{Source} \cdot I_{Source}} \tag{1}$$

Another efficiency is directly related to PPC operation, which is the *Converter efficiency* (η_{conv}), defined in (2) [4], where (V_{in}, V_{out}) are the input and output voltages of the converter, respectively, and (I_{in}) is the current entering the converter, while (I_{out}) is the current leaving the converter. The sign convention indicates power flow through the converter; that is, current entering through the positive terminal indicates power flow *into* the converter, while current flowing out of a positive terminal indicates power flowing out of the converter.

$$\eta_{conv} = \frac{P_{out}}{P_{in}} = \frac{V_{out} \cdot I_{out}}{V_{in} \cdot I_{in}} \tag{2}$$

The nature of PPC converter operation requires the definition of another attribute, which is the *processed power ratio* (K_{pr}), presented in Equation (3). K_{pr} defines the ratio of the power processed by the converter (P_{conv}) to the overall power drawn from the source (P_{Source}) [4,13,14].

$$K_{pr} = \frac{P_{conv}}{P_{source}} = \frac{V_{out} \cdot I_{out}}{V_{source} \cdot I_{source}} \tag{3}$$

In addition to the previous equations, the *static voltage gain* (G_V) is also a key parameter in defining PPC operation, given in Equation (4) [6,15–17].

$$G_V = \frac{V_{Load}}{V_{Source}} \tag{4}$$

It is worth mentioning that this work considers G_V to be always positive, i.e., $G_V \geq 0$, since negative values in a given topology (indicating a *reversed* source or load) will be equal (i.e., absolute) or refer to another topology, as will be seen in Section 3.

The *stress factor* coefficients provide a quantitative approach to evaluate and compare converter designs (*topology*) [15,18–20], independently of their power ratings. The three main components of any power converter are *semiconductor switches*, *magnetic windings*, and *capacitors*. The stress factor calculations can be simplified assuming a lossless converter (i.e., $\eta_{conv} = 100\%$) and further assuming a large enough inductor to suppress any ripple current [15]. Equations (5)–(7) relate to the Semiconductor Stress Factor (SCSF), Winding Stress Factor (WSF), and Capacitor Stress Factor (CSF), respectively [21,22].

$$SCSF_i = \frac{\sum_j W_j}{W_j} \cdot \frac{V_{max\ SC}^2 \cdot I_{rms\ SC}^2}{P_{in}^2} \tag{5}$$

$$WSF_i = \frac{\sum_j W_j}{W_j} \cdot \frac{V_{max\ L}^2 \cdot I_{rms\ L}^2}{P_{in}^2} \tag{6}$$

$$CSF_i = \frac{\sum_j W_j}{W_j} \cdot \frac{V_{max\ C}^2 \cdot I_{rms\ C}^2}{P_{in}^2} \tag{7}$$

$$V_{max\ L} = \sum_i D_i \cdot |V_i| \tag{8}$$

where W_j is the weight factor of the jth component and can be considered 1 as a starting point [18], and $V_{max\ SC}$, $V_{max\ C}$ are the maximum voltages seen or *blocked* by the semiconductor switch and the capacitor, respectively. $I_{rms\ SC}$, $I_{rms\ L}$, and $I_{rms\ C}$ stand for the *root-mean-square* current passing through the semiconductor switch, the capacitor, and the inductor. P_{in} is the input power to the converter and D_i is the duty of the ith cycle. $V_{max\ L}$ is the maximum voltage seen by the magnetic component (i.e., inductor). $|V_i|$ is the absolute value of the winding voltage in the ith operating state [18].

After developing the stress factor for each single component, the *global* stress factor for all semiconductors, capacitors, and inductors can be summed as in (9)–(11).

$$SCSF = \sum_i SCSF_i \tag{9}$$

$$WSF = \sum_i WSF_i \tag{10}$$

$$CSF = \sum_i CSF_i \tag{11}$$

Among the reviewed literature, several papers have implemented the component stress factor to evaluate their topologies and differentiate their performance in various operations. Chao [23] has demonstrated an inverse relation between stress factors and the turn ratio in their IPOS and ISOP PPC converters. Values well below 0.01 were reported in [15] for all SCSFs, WSFs, and CSFs. To have perspective, ref. [24] reported figures larger by *orders of magnitude* for the component stress factors.

The work of Zeintarski et al. [25] illustrates the component stress factors over a range of G_V for two proposed PPCs: the Full-Bridge Series-Connected Partial Power Processor (FBSPPC) and the Full-Bridge Push-Pull Series-Connected Partial Power Processor (FBPPSPPC). Both topologies show a reduction in component stress factors with G_V values approaching unity.

Load power P_{Load} also has a direct impact on the component stress factors, where it is observed in [20] that increasing P_{Load} will lead to larger stress on components in the case of a full-power rated converter compared to PPC.

Lastly, *non-active power* (N) is the energy stored in the reactive element (capacitor or inductor) and not transferred from the input to the output of a DC-DC converter operating in the steady state [2,20], defined also in Institute of Electrical and Electronics Engineers (IEEE) standard 1459 [26] and measured in Volt-Ampere Reactive (VAR). Inductor non-active power (N_L) and capacitor non-active power (N_C) are evaluated by (12) and (13), where E_L and E_C are the energy stored in inductor and capacitor in joules, D is the dimensionless duty cycle of each switching period T_s. $v(t)$ and $i(t)$ are the instantaneous voltage and current.

$$N_L = \frac{2 \cdot \Delta E_L}{T_s} = \frac{2 \cdot \int_0^{D \cdot T_s} |v_L(t) \cdot i_L(t)| dt}{T_s} \tag{12}$$

$$N_C = \frac{2 \cdot \Delta E_C}{T_s} = \frac{2 \cdot \int_0^{D \cdot T_s} |v_C(t) \cdot i_C(t)| dt}{T_s} \tag{13}$$

$$F = \frac{P_{conv}}{\sqrt{P_{conv}^2 + (N_C + N_L)^2}} \tag{14}$$

Equation (14) represents the *Fryze* power factor (F), which defines the ratio of non-active to active power [2]. It also contributes to the converter power losses [27] and requires over-sizing the components, although it does not contribute to the transfer of real power. Isolated topologies show a direct influence of the transformer *turn ratio* (n) to the Fryze power factor. For a given topology, G_V will have a direct impact.

Figure 2 indicates how the *Fryze* power factor can be affected by different topologies and operation modes. Both the Symmetrical Half-Bridge Current-Fed Power Processor (SHBCFPP) and Full-Bridge Phase-Shift Current-Fed Power Processor (FBPSCFPP) appear in the work of [2] as prototypes rated for 2200 W. The FBSPPC and FBPPSPPC are 225 W and 112.5 W, respectively, presented by Zientarski et al. in [25].

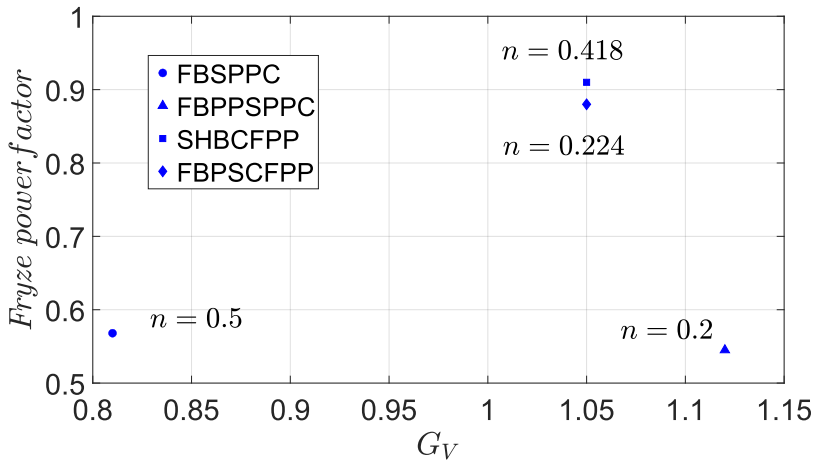

Figure 2. Fryze power factor for different topologies of *isolated* PPC operating at different G_V.

3. Isolated PPP Architectures

The required isolation refers solely to the converter topology, since a galvanic path will exist between the system's input and output. Non-isolated converters cannot be used in these topologies due to two main constraints: the inherited risk of short-circuit and the fact that a non-isolated converter will end up processing full power [28]. A workaround to overcome those shortfalls will be revised in Section 4.1.

As commented earlier, PPC deals with a new way to connect power converters. At first glance, such connections might be misleading in that they influence different topologies. Based on the work of [28], it is proposed to use the concept of a *dummy converter* as a systematic approach for segregating and evaluating all possible architectures.

Figure 3 illustrates the three main connection groups, i.e., PISO, SIPO, and ISOS. IPOP is left out as it represents a specific case study that will be commented on in Section 3.7.

The dashed connection boxes in the same figures indicate the possibility of a variety of connections, which will be examined in the subsequent sections. In accordance with the assigned notations, the power is transferred from the *source* side into the *load* side; hence, the DC current flow is fixed in Figure 3 to indicate leaving the source and entering in the load.

3.1. Input-Parallel-Output-Series Topology (IPOS)

By consulting Figure 3a, and ensuring that V_{in} is equal to V_{Source}, four generic connections can be derived. Figure 4 presents the three possible connections while highlighting the *series* connection between the two converters (in red) and the *parallel* connection of V_{Source} to V_{in} (in blue). The fourth connection is shaded out as it is not realizable, as will be discussed in the upcoming part.

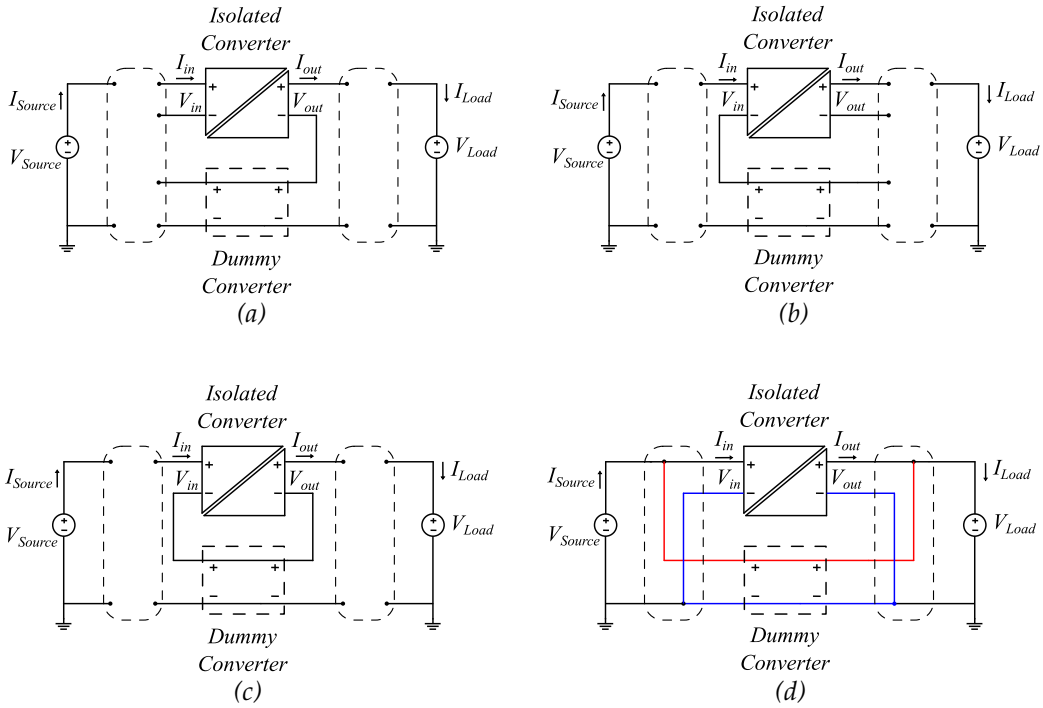

Figure 3. PPC configurations: (**a**) Isolated converter's *output* connected in *series* with the dummy converter's *output* to produce IPOS topology. (**b**) *Series* connection between the *input* of the isolated converter and the *input* of the dummy converter to produce ISOP topology. (**c**) Series connections for both sides of the isolated and dummy converters giving rise to ISOS topology. (**d**) IPOP diagram showing *source* connected in parallel to the *load*, which will be analyzed further in Section 3.7.

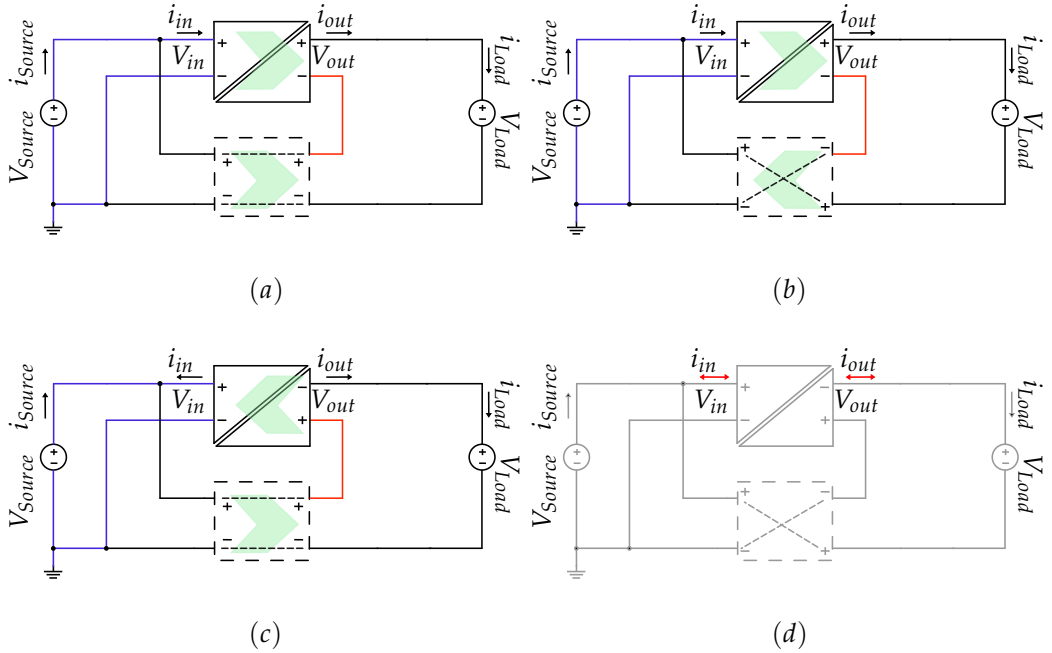

Figure 4. IPOS configurations: (**a**–**c**) are three realizable variants of IPOS topology, and (**d**) is the fourth analytical case, not achievable in reality. The arrow inside the *dummy converter* indicates the *direct* power flow, while the arrow inside the *isolated converter* indicates the power flow within the converter itself. Note the sign change of the converters.

Writing the equations of V_{source} and V_{Load} as functions of V_{in} and V_{out} can further simplify the interactions between the different topologies. The equations are tabulated in Table 1, showing that V_{in} is held to V_{Source} and the three possibilities of V_{Load}.

Revisiting the voltage equations in Table 1, another feature can be deduced. The V_{Load} equation in Figure 4a indicates that the system will have overall *step-up* operation, although the converter itself can be either step-up or step-down; hence, several literature sources refer to this topology as *step-up* [2,4,29]. Following the same analysis for the V_{Load} equation in Figure 4b, it shows that it requires a step-up converter to prevent a negative V_{Load}; if the converter is *step-down*, it will lead to *negative* load voltage. The third case, i.e., Figure 4c, needs a step-down converter to maintain a positive V_{Load}; otherwise, it will lead to *negative* voltage on the load.

Table 1. Summery of IPOS equations.

Source	Load	Connection Diagram from Figure 4
$V_{Source} = V_{in}$	$V_{Load} = V_{in} + V_{out}$	(a)
$V_{Source} = V_{in}$	$V_{Load} = -V_{in} + V_{out}$	(b)
$V_{Source} = V_{in}$	$V_{Load} = V_{in} - V_{out}$	(c)
$I_{Source} = I_{in} + I_{out}$	$I_{Load} = I_{out}$	(a)
$I_{Source} = -I_{in} + I_{out}$	$I_{Load} = I_{out}$	(b)
$I_{Source} = I_{in} - I_{out}$	$I_{Load} = I_{out}$	(c)

Analyzing the last case by applying Kirchoff's Voltage Law (KVL) shows $V_{Load} = -V_{in} - V_{out}$, or in other words, a negative G_V. By trying to apply the same approach to circuit (d) in Figure 3, if the designated I_{Load} is kept in the direction to flow into V_{Load}, it has to leave the partial converter from the negative terminal. Following the path of I_{Load}, it will leave the negative terminal of the load and enter the positive terminal of the dummy converter's output. Flowing directly through the dummy converter, I_{Load} will leave from the input side's positive terminal, which means it has to join I_{Source}, and both of them enter the partial converter. This case implies positive power flow (consumption) by both ends of the partial converter, which is unrealizable.

The above features can be illustrated by deriving the relations between the different voltages in terms of K_{pr} and G_V [11,15,30]. Equations (15)–(17) refer to the topologies of Figure 4a,b,c, respectively. Equation (18), however, is developed to further provide a mathematical proof of the *unviability* of the circuit in Figure 4d, since it will develop a *negative* power processing ratio.

$$K_{pr_a} = \eta_{sys} - \frac{\eta_{sys}}{G_V} \tag{15}$$

$$K_{pr_b} = \eta_{sys} + \frac{\eta_{sys}}{G_V} \tag{16}$$

$$K_{pr_c} = \frac{\eta_{sys}}{G_V} - \eta_{sys} \tag{17}$$

$$K_{pr_d} = -\eta_{sys} - \frac{\eta_{sys}}{G_V} \tag{18}$$

The above equations can be further visualized in Figure 5. Referring back to the IPOS (a) V_{Load} formula in Table 1, it can be seen that V_{Load} will always be bigger than V_{Source}; hence, G_V is always $\geq$1, and this achieves overall *step-up* operation, and IPOS (a) cannot operate in scenarios where V_{Load} is set lower than V_{Source}. IPOS (b), on the other hand, can work throughout the entire range of G_V, which can be translated as having *negative* V_{Load} (i.e., swapped). However, *negative* K_{pr} values appear when operating $-1 < G_V < 0$. This can be interpreted as having power flowing in the *reverse* direction through the converter. Another feature that can be concluded about IPOS (b) is that the majority of power will be processed by the converter, and the converter will never process less than 50% of the total input power.

To realize IPOS (c), V_{Load} will always be lower than V_{Source}, as seen in Table 1, and it can also have negative values (*reverse* connected). This operation mode produces an overall *step-down* operation for positive values of K_{pr}.

The last case of IPOS (d) is only plotted for integrity, but it is rendered inapplicable, as seen earlier.

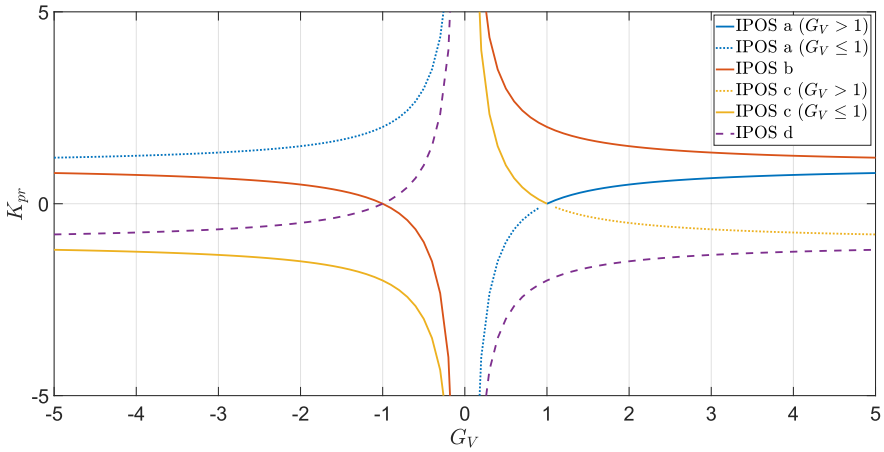

Figure 5. IPOS $K_{pr}(G_V)$: IPOS (a) based on (15), with the part of $G_V < 1$ shaded out. IPOS (b) from (16). IPOS (c) from (17) with $G_V > 1$ shaded out. IPOS (d) was plotted to maintain the review integrity.

3.2. IPOS-Based Converters

An example of Figure 4a is a step-down Dual Active Bridge (DAB) operation that can be seen in the work proposed by Mishra et al. [31] as a battery emulator based on a DAB converter with step-up IPOS topology. Although the DAB was utilized, the authors commented that a common-mode circulation current will be flowing between the input and the output of the converter systems, which requires further study. Analytical work performed by the authors shows that the η_{sys} is always higher than the η_{conv}.

Omar et al. [14] utilized a *current-fed dual-inductor push–pull* in step-up formation, also coinciding with Figure 4a. The authors state the main advantage is *soft switching*. The proposed design of the converter also permits reverse power flow; however, this operation mode was not analyzed in their work.

Zapata et al. [11] used a single flyback converter, which is claimed to have reduced current ripple at the input and divided the individual converters' power ratings. Table 2 summarizes the salient features of the reviewed systems, while Figure 6 illustrates some designs from the literature.

Table 2. Reviewed IPOS-based PPC.

Reference	Converter	Topology	K_{pr}	G_V	Application	System Power [kW]	η_{sys} [%]
[31]	DAB	IPOS (a)	40%	1.73	Battery emulator	0.10	99.90
[14]	Dual-inductor push–pull	IPOS (a)	25%	13.3	PV	1.20	99.00
[28]	Flyback	IPOS (a)	41%	1.43	PV	0.10	95.50
[16]	Flyback	IPOS (a)	44%	1.99	PV	0.10	98.50
[32]	DAB	IPOS (a)	44%	3.00	Battery charging	0.72	95.60
[11]	Flyback	IPOS (a)	20%	1.17	PV	0.99	90.00
[33]	Buck-boost Full-bridge	IPOS (b)	<40%	<3.5	PV	1.80	98.90
[34]	Full bridge push–pull	IPOS (a)	20%	0.99	Battery charging	22.00	99.0
[35]	Full bridge phase shift	IPOS (a)	20%	<1.0	PV	78.00	98.5

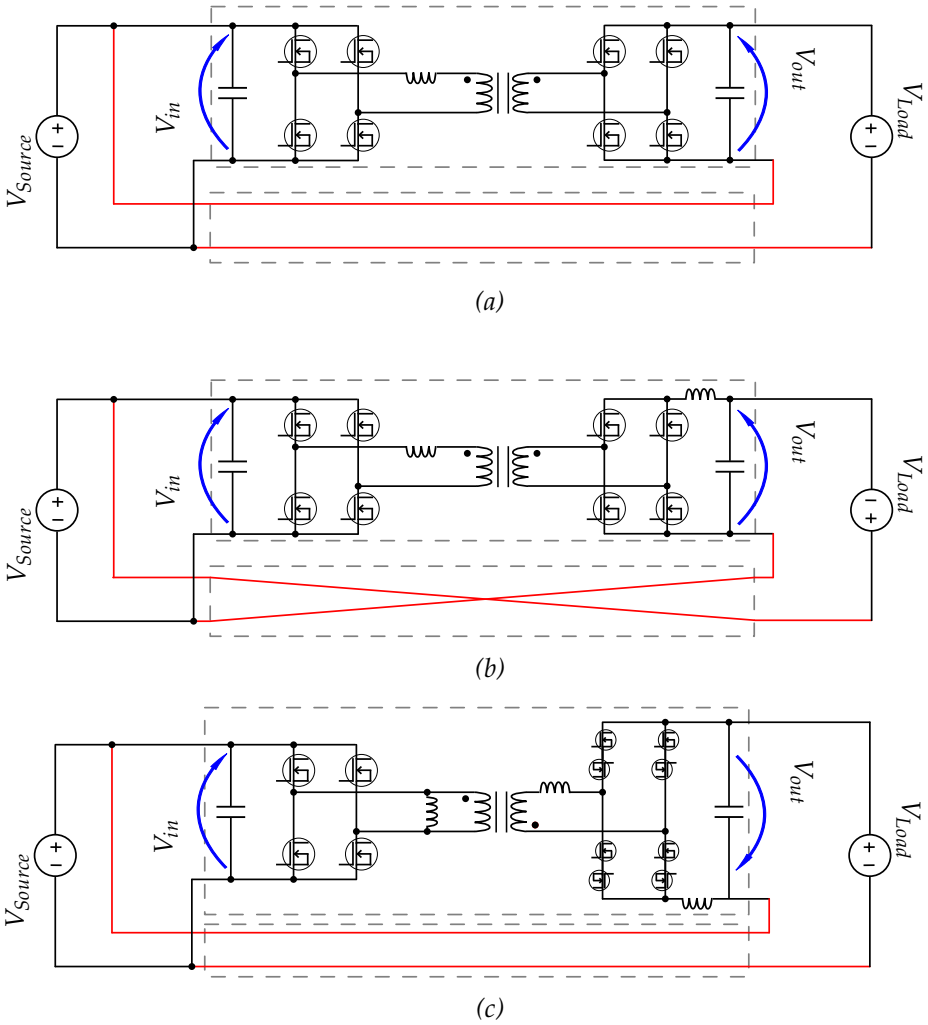

Figure 6. Examples of IPOS topologies in the literature: (**a**) IPOS-a topology implemented in [31]. (**b**) IPOS-b seen in work of Liu et al. [15], with *reversed* V_{Load}. (**c**) IPOS-c topology from [33]; notice the *reversed* V_{out} arrow to indicate flipped output.

The DAB converter in Figure 6a has its input connected to V_{Source}, while its output is connected in series to V_{Source}, and both are connected to V_{Load} to give a straightforward example of the IPOS (a) case.

The outstanding feature of Figure 6b is that the authors *reversed* the V_{Load}. Carrying out KVL around the circuit yields $V_{Load} + V_{out} - Vin = 0$, while if the load was wired as designated, it would yield IPOS (b).

Figure 6c demonstrates another attribute, which is the *reversed* V_{out}. The right-hand side of the converter was *flipped* so that the negative of the converter's output is connected to the positive side of the load, thus fulfilling the IPOS (c) topology.

As it can be seen from [16,20,29,33], for example, the PPC efficiency holds high values throughout a wide range of operating conditions, contrary to the full-power converter, which achieves high efficiency generally at a specific operating point.

3.3. Input-Series-Output-Parallel Topology (ISOP)

Applying the same systematic approach of the previous Section 3.1 to the ISOP topology demonstrated in Figure 3b, four connections can be derived, as demonstrated in Figure 7.

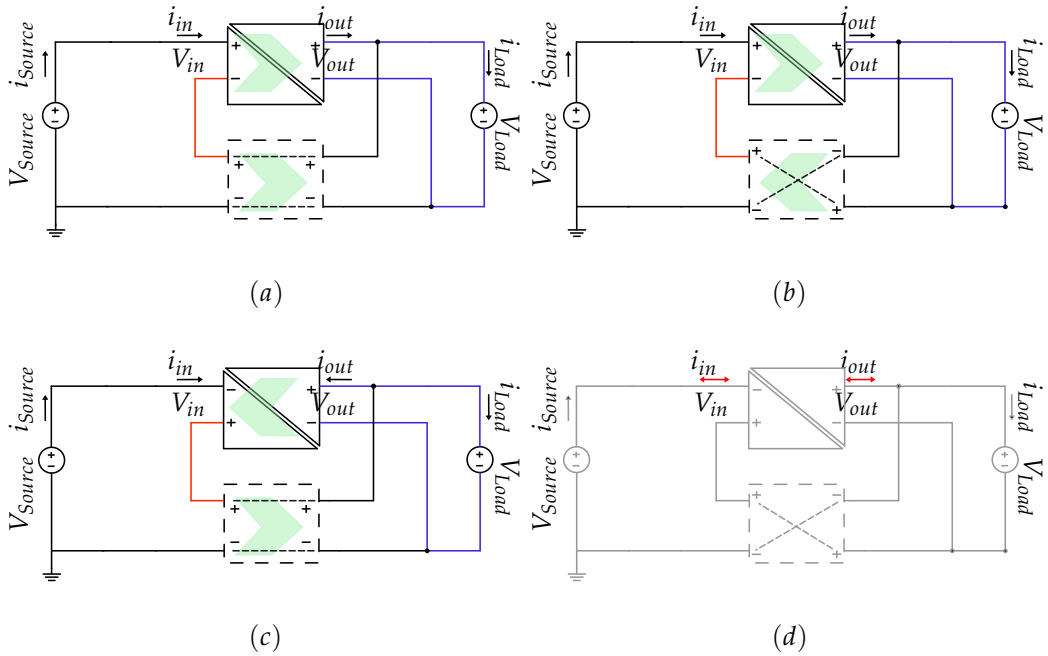

Figure 7. ISOP configurations: (**a**–**c**) are three realizable variants of ISOP topology, and (**d**) is the fourth analytical case, not achievable in reality. The arrow inside the dummy converter indicates the direct power flow, while the arrow inside the isolated converter indicates the power flow within the converter itself. Note the sign change of the converters.

Table 3 contains a summary of the equations describing the behavior of each topology. By utilizing the definition of η_{sys} and G_V, Equations (19)–(21) are developed relevant to the topologies in Figure 7a,b,c, respectively.

Table 3. Summery of ISOP equations.

Source	Load	Connection Diagram from Figure 7
$V_{Source} = V_{in} + V_{out}$	$V_{Load} = V_{out}$	(a)
$V_{Source} = V_{in} - V_{out}$	$V_{Load} = V_{out}$	(b)
$V_{Source} = -V_{in} + V_{out}$	$V_{Load} = V_{out}$	(c)
$I_{Source} = I_{in}$	$I_{Load} = I_{in} + I_{out}$	(a)
$I_{Source} = I_{in}$	$I_{Load} = I_{in} - I_{out}$	(b)
$I_{Source} = I_{in}$	$I_{Load} = -I_{in} + I_{out}$	(c)

$$K_{pr_a} = \eta_{sys} - G_V \tag{19}$$

$$K_{pr_b} = G_V - \eta_{sys} \tag{20}$$

$$K_{pr_c} = G_V + \eta_{sys} \tag{21}$$

$$K_{pr_d} = -G_V - \eta_{sys} \tag{22}$$

By plotting the Equations (19)–(22), Figure 8 can visualize the behavior of each ISOP topology. Starting with the ISOP (a) curve, it is seen that G_V is bounded between 1 and 0, since V_{Source} will always be bigger than V_{Load}, so $G_V < 0$ is not realizable. The ISOP (b) and (c) topologies can operate throughout the whole range of G_V (including negative source voltage) with linear characteristics. ISOP (d) is also plotted in Figure 8 for review integrity, but it will not be practically achievable. One of the advantages of ISOP topology is that it reduces stress on semiconductor switches in high voltage applications [36].

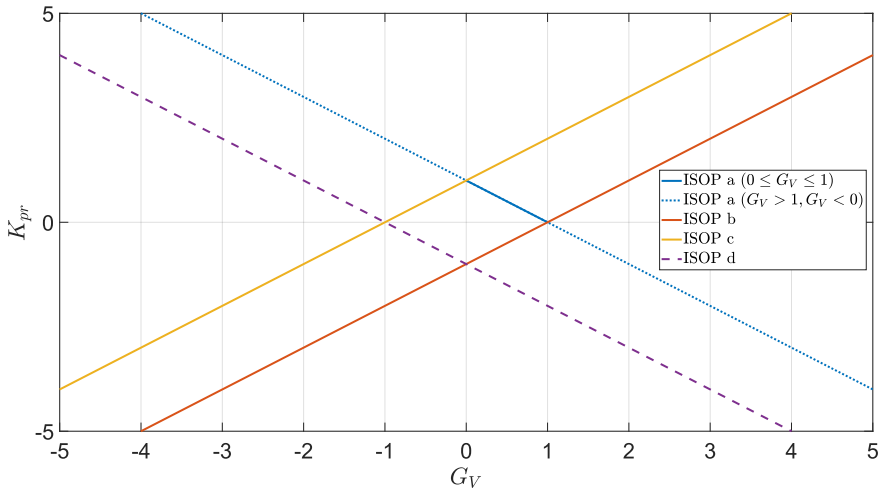

Figure 8. ISOP $K_{pr}(G_V)$: ISOP (a) topology trend from (19) with $G_V > 1$ shaded out. ISOP (b) trend (20) and $G_V < 1$ shaded out. ISOP (c) trend from (21). ISOP (d) was plotted in this figure as another graphical proof that K_{pr} will be negative over the whole range of operation, hence rendering this mode invalid.

3.4. ISOP-Based Converters

The work of Tao, Wang, and Zhuo [13] demonstrated using a *CLLC* converter to achieve *four-quadrant* operation. Their work is based on ISOP (a), providing bi-directional power flow between a DC bus and a battery of either a higher or lower voltage.

Renaudineau et al. [37] implemented ISOP (b) to generate *rectified* sinusoidal DC from a PV string input. In their simulation, they mitigated the harmonics content by relieving the inverter from high-frequency switching and dedicating it to *unfolding* only.

In [38], Anzola, Aizpuru, and Arruti proposed ISOP (a) for EV fast charging applications. Their simulation shows a steep drop of N_L and N_C as the State of Charge (SOC) builds up. A *down-scaled* prototype pf the PPP demonstrates a reduction of 65% in the size of the magnetic components, i.e., the transformer and inductor, when compared to the full power converter.

Table 4 displays a comparison between the reviewed ISOP systems, while Figure 9 presents examples of ISOP topologies.

Table 4. Reviewed ISOP-based PPC.

Reference	Converter	Topology	K_{pr}	G_V	Application	System Power [kW]	η_{sys} [%]
[13]	H-bridge+CLLC	ISOP (a)	16%	1.00	Battery	45.0	97.91
[39]	DAB	ISOP (a)	25%	0.75	EV	1.00	97.00
[16]	isolated full-bridge	ISOP (a)	13%	0.84	PV	0.82	98.50
[16]	Full-bridge	ISOP (b)	11%	1.10	PV	1.00	97.50
[38]	DAB	ISOP (a)	19%	0.45	Battery	2.20	99.62
[40]	Integrated full-bridge	ISOP (a)	25%	0.75	PV	2.0	98.60
[37]	Full-bridge	ISOP (a)	12%	0.89	PV	3.30	97.50
[28]	Flyback	ISOP (c)	58%	1.40	PV	0.10	92.00

Figure 9a represents a DAB-based ISOP (a) topology, where V_{Load} is connected in parallel to V_{out} of the converter, while the same (i.e., V_{Load}) is connected in series to V_{in}, and then the sum of both voltages is connected to V_{Source}.

ISOP (b) topology is demonstrated in Figure 9b, where the flayback converter's output is connected in parallel to V_{Load}, while its input voltage is connected in series between its output voltage and the source.

The full-bridge converter displayed in Figure 9c displays an *inverted* left-hand side, where the negative side of V_{in} is connected to the positive side of V_{Source}.

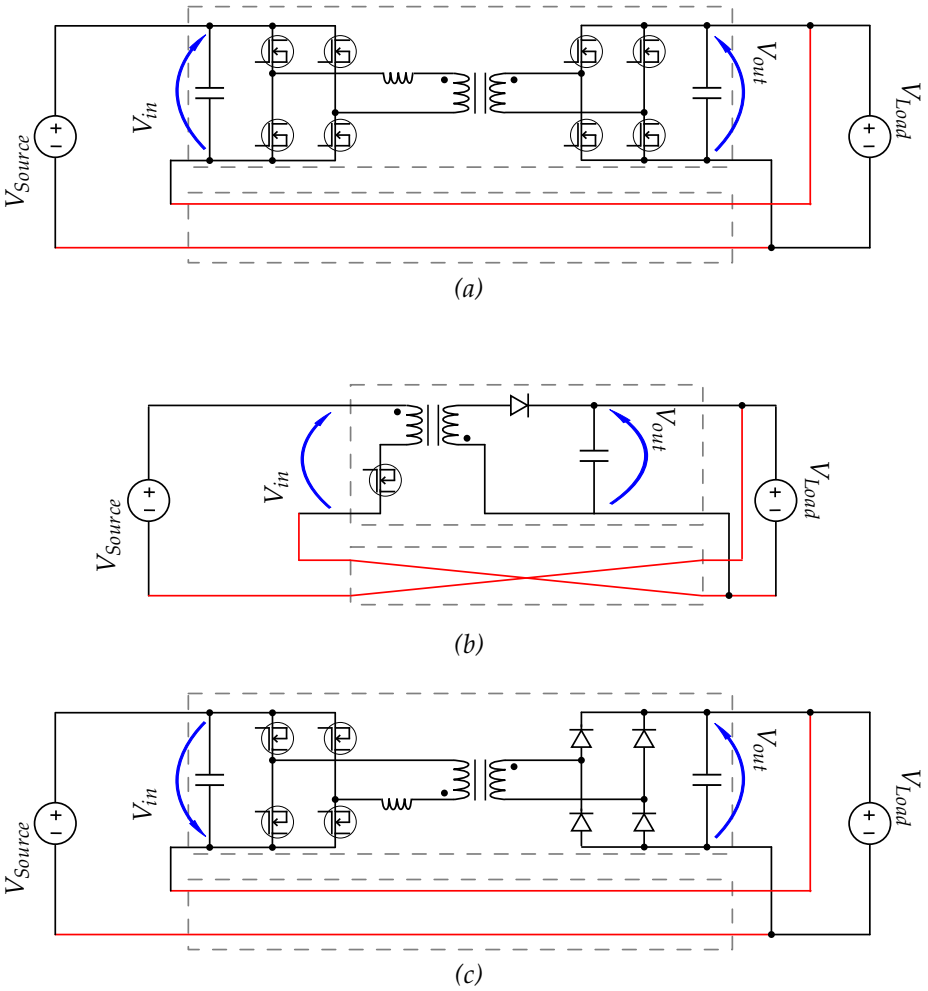

Figure 9. Examples of ISOP in the reviewed literature: (**a**) DAB-based ISOP (a) from [39]. (**b**) ISOP (b) flyback. (**c**) ISOP (c) integrated full bridge [37]; note the *inverted* V_{in}.

3.5. Input-Series-Output-Series Topology (ISOS)

One more configuration can be deduced in the isolated topology group, which is Input-Series-Output-Series (ISOS). Figure 10 displays all the four combinations. By examining Figure 10a, the series connection (marked in red) can be seen on both sides of the input and the output.

By developing the power balance of the converter (for an *ideal* converter) in (23) with the aid of the current equations in Table 5, it can be seen that topologies (b) and (c) in Figure 10 are not achievable.

$$P_{in} = P_{out} \tag{23}$$

$$V_{in} \cdot I_{in} = V_{out} \cdot I_{out} \tag{24}$$

However, since $I_{in} = -I_{out}$, I_{out} has a *reversed* direction in comparison to the designated direction in Figure 10b. This negative current reflected in (24) leads to a net positive power pouring into the converter, turning the converter into one that *sinks* power instead of *transferring* it.

A similar case can be deduced in the topology of ISOS (c); however, this time V_{out} has a *reversed* sign but still leads to the same conclusion of the converter ending up sinking power. These observations halt any further study of those two arrangements.

On the other hand, in Figure 10d, the current will flow out of the positive terminals of the *Load* and *Source* as well, which is not a valid power transfer mode.

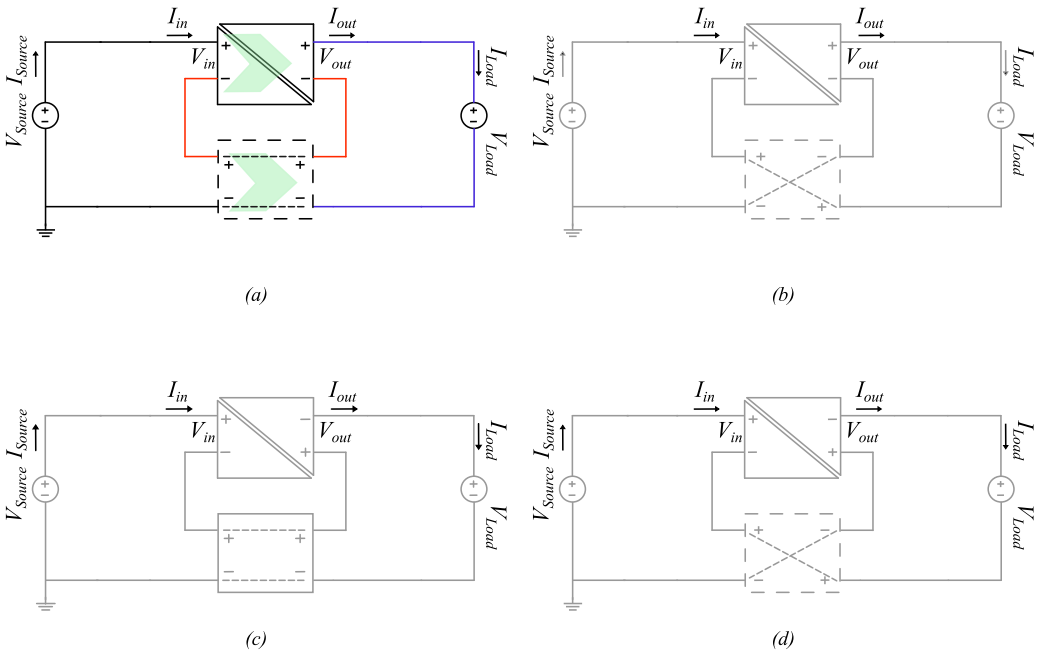

Figure 10. ISOS configurations: (**a**,**d**) are two realizable variants of ISOS topology, while (**b**,**c**) are analytical cases not achievable in reality. The arrow inside the *dummy converter* indicates the *direct* power flow, while the arrow inside the *isolated converter* indicates the power flow within the converter itself. Note the sign change of the converters.

An attempt to *flip* the *Load* terminals in Figure 10d will end up yielding an identical topology to Figure 10a.

Maintaining the analysis method used in Sections 3.1 and 3.3, the ISOS equations can be derived and summarized in Table 5.

Table 5. Summary of ISOS equations.

Source	Load	Figure 10 Diagram	Viability
$V_{Source} = V_{in} - V_{out} + V_{Load}$	$V_{Load} = V_{Source} - V_{in} + V_{out}$	(a)	yes
$V_{Source} = V_{in} + V_{out} - V_{Load}$	$V_{Load} = -V_{Source} + V_{in} + V_{out}$	(b)	no
$V_{Source} = V_{in} + V_{out} + V_{Load}$	$V_{Load} = V_{Source} - V_{in} - V_{out}$	(c)	no
$V_{Source} = V_{in} - V_{out} - V_{Load}$	$V_{Load} = -V_{Source} + V_{in} - V_{out}$	(d)	no
$I_{Source} = I_{in} = I_{out} = I_{Load}$	$I_{Load} = I_{in} = I_{out} = I_{Source}$	(a)	yes
$I_{Source} = I_{in} = -I_{out} = -I_{Load}$	$I_{Load} = -I_{in} = I_{out} = -I_{Source}$	(b)	no
$I_{Source} = I_{in} = I_{out} = I_{Load}$	$I_{Load} = I_{in} = I_{out} = I_{Source}$	(c)	no
$I_{Source} = I_{in} = -I_{out} = -I_{Load}$	$I_{Load} = -I_{in} = I_{out} = -I_{Source}$	(d)	no

Deriving K_{pr} in terms of G_V produces an extra term in Equation (25). This term is represented by the ratio of V_{in} to V_{Load}, and its effect will further be commented on in the upcoming Section 3.6.

$$K_{pr} = \left(\frac{V_{in}}{V_{Load}}\right) G_V + \eta_{sys} - 1 \tag{25}$$

By plotting Equation (25) for several values of V_{in}/V_{Load} as in Figure 11, the generic trends and the influence of V_{in}/V_{Load} ratio can be seen.

The trends in Figure 11 imply the necessity to hold V_{in}/V_{Load} at a steady value to maintain proper and predictable operation of the system.

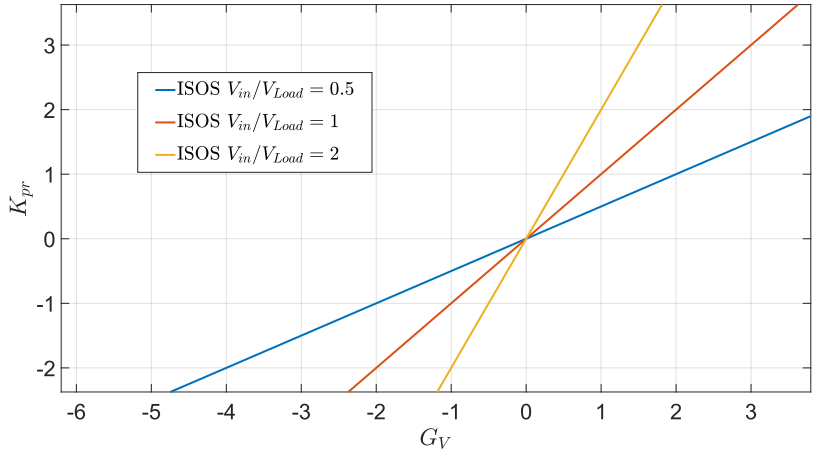

Figure 11. ISOS $K_{pr}(G_V)$: Linear relation between K_{pr} and G_V at different V_{in}/V_{Load} ratios.

3.6. ISOS-Based Converters

Within the surveyed and reviewed literature, the ISOS topology was the least encountered. The work seen in [41] contains an intermediate ISOS, utilized as a *Half DC Bus Boost Converter*, but no further details about its performance characteristics were developed. Ref. [42] described two converters connected in ISOS formation, with one of them having a 1:1 ratio, which can be thought of as the dummy converter stated earlier; however, it is introduced to achieve full galvanic isolation.

The work of Lopusina and Grbovic [43] illustrates explicitly an ISOS-topology converter; nevertheless, it is based on a *non-isolated* converter and hence will be seen in the upcoming Section 4.2.

3.7. Input-Parallel-Output-Parallel Topology (IPOP)

This arrangement represents a special case, since two out of its four variants will lead to short-circuiting the source with the load, leaving these scenarios out of the analysis. In the other two cases, V_{Source} will always be connected in parallel to V_{Load}, which leads to unity G_V as expressed in (26).

$$K_{pr}(G_V) = 1 \tag{26}$$

Furthermore, $|V_{in}| = |V_{out}|$ can be seen in Figure 12, where cases (b) and (d) are also greyed out due to short-ciruits.

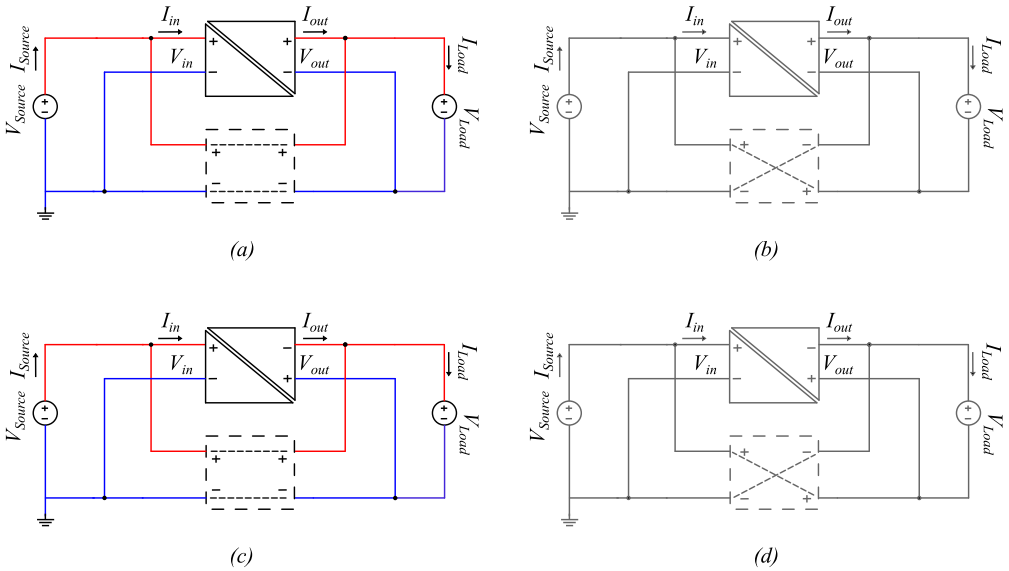

Figure 12. IPOP combinations: (**a**,**c**) *might* share load current. (**b**,**d**) will cause short-circuits.

Although cases (a) and (c) in Figure 12 theoretically exist, their practical applications might not be of much interest due to the fact that V_{Load} is held steady to V_{Source}. Such fundamental restrictions limited the interest in further research on this type of topology, and therefore no related literature was found.

4. Non-Isolated PPP Architectures

Revisiting the topologies developed in the previous parts (Sections 3.1 and 3.3), it can be seen that some topologies actually will not suffer from the short-circuit mentioned at the beginning of Section 3 when using non-isolated converters. Ref. [21] analytically developed all possible combinations for such arrangements, and based on that work, further analysis of operation is carried out in the following subsection. For simplicity purposes, this work will assume the use of a DC-DC *boost* converter, such as the one shown in Figure 13. Nevertheless, the analysis remains the same for any other type of non-isolated converter being used.

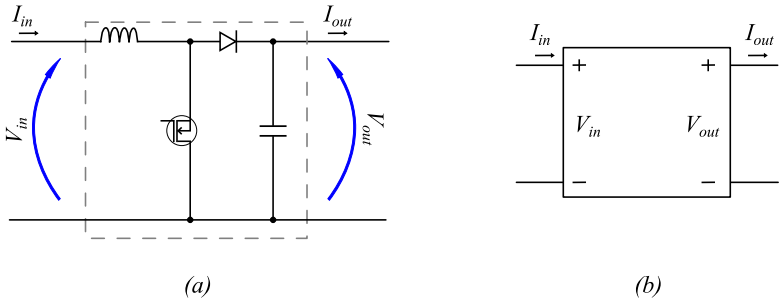

Figure 13. (**a**) Boost converter. (**b**) Block representation.

4.1. Fractional Topology

Looking back into the IPOS topologies demonstrated in Figure 4, it can be seen that for configuration IPOS (b), the negative terminal on each of the ports of the converter is actually connected to the same node. The same observation can also be seen in configuration ISOP (b) in Figure 7, as was already demonstrated for ISOS in Section 3.6. Such a remark means that a non-isolated converter can be connected directly in those topologies, where Figure 14 demonstrates the possible combinations of such non-isolated PPP topologies.

On the other hand, ref. [28] suggested solving the short-circuit problem by simply *inverting* the converter terminals. Figure 14c,d illustrate inverted boost converter connections. Such topologies are referred to in the literature as the Fractional Power Converter (FPC) [6]. It is to be noted that such configurations might lead to loss of partial power processing, as seen in [28]. The *Active Voltage Balancer* seen in Figure 14e is just one proposed arrangement, as seen in [44]; other arrangements might be proposed.

The voltage and current equations are stated again in Table 6 for easy reference; however, the same equations were already developed in Table 1 for IPOS (b), and Table 3 for ISOP (b).

Table 6. Summery of non-isolated PPP equations.

Source	Load	Connection Diagram from Figure 14
$V_{Source} = V_{in}$	$V_{Load} = -V_{in} + V_{out}$	(a)
$V_{Source} = V_{in} - V_{out}$	$V_{Load} = V_{out}$	(b)
$V_{Source} = V_{in}$	$V_{Load} = -V_{in} + V_{out}$	(c)
$V_{Source} = V_{in} - V_{out}$	$V_{Load} = -V_{out}$	(d)
$V_{Source} = V_{in} - V_{out} + V_{Load}$	$V_{Load} = V_{Source} - V_{in} + V_{out}$	(e)
$I_{Source} = I_{in} + I_{out}$	$I_{Load} = I_{out}$	(a)
$I_{Source} = I_{in}$	$I_{Load} = I_{out} - I_{in}$	(b)
$I_{Source} = I_{in} + I_{out}$	$I_{Load} = I_{out}$	(c)
$I_{Source} = I_{in}$	$I_{Load} = I_{in} + I_{out}$	(d)
$I_{Source} = I_{in} = I_{out} = I_{Load}$	$I_{Load} = I_{in} = I_{out} = I_{Source}$	(e)

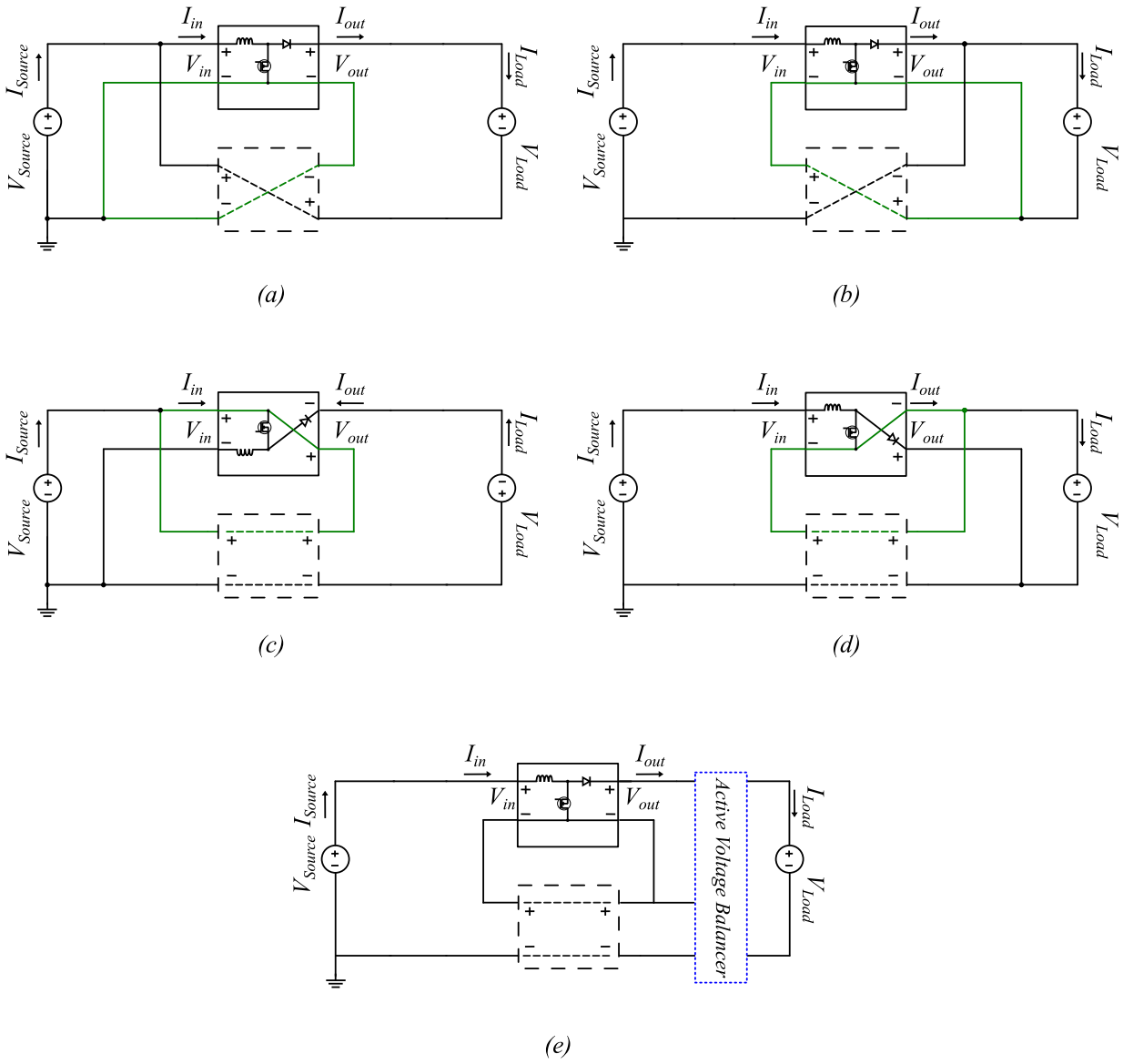

Figure 14. Realizable variants of non-isolated PPP topologies: (**a**) IPOS-b non-inverted. (**b**) ISOP-b non-inverted. (**c**) IPOS-c inverted. (**d**) ISOP-c non-inverted. (**e**) ISOS non-inverted. The *green* path represents a redundant loop.

Equations (16), (20), and (25) remain valid to represent K_{pr} as a function of G_V for non-isolated IPOS-b, ISOP-b, and ISOS-a, respectively.

4.2. Fractional Topology-Based Converters

Due to the recent interest in the applications of non-isolated PPP, only a few examples could be found in the reviewed literature where an explicit non-isolated converter is used [4,29]. Kim and Parkhideh [45] presented a comparison between non-isolated and isolated converters for PVs and battery applications, where they stated higher efficiency for isolated PPC. The work presented in [6], based on the proposed *Modified Inductor Boost Converter* in [46], states that a K_{pr} of less than 25% is achieved for a power conversion system of 750 W. The proposed topology in this work follows case (c) in Figure 14.

Another example can be found in the analytical and simulation work of the *Cuk-based* PPP converter in [47] connected according to case (a) in Figure 14. The authors suggested several *Cuk*-based converter topologies. However, no values were given about operating K_{pr} or G_V.

In [48], the authors studied several scenarios of boost, buck, and buck–boost converters in the ISOS formation. A buck–boost prototype was implemented in the configuration of case (d) to develop a battery charger of 1.2 kW.

The arrangement presented by [43] and demonstrated in Figure 15c has several salient points to be commented on. Firstly, it treats the voltage ratio V_{in}/V_{Load} mentioned earlier in Section 3.5 by using an *Active Voltage Balancer* that transfers bipolar DC into unipolar [44], and it is used to stabilize the *Load* voltage. The selected topology for the Active Voltage Balancer is a Series Resonant Balancer Converter (SRBC).

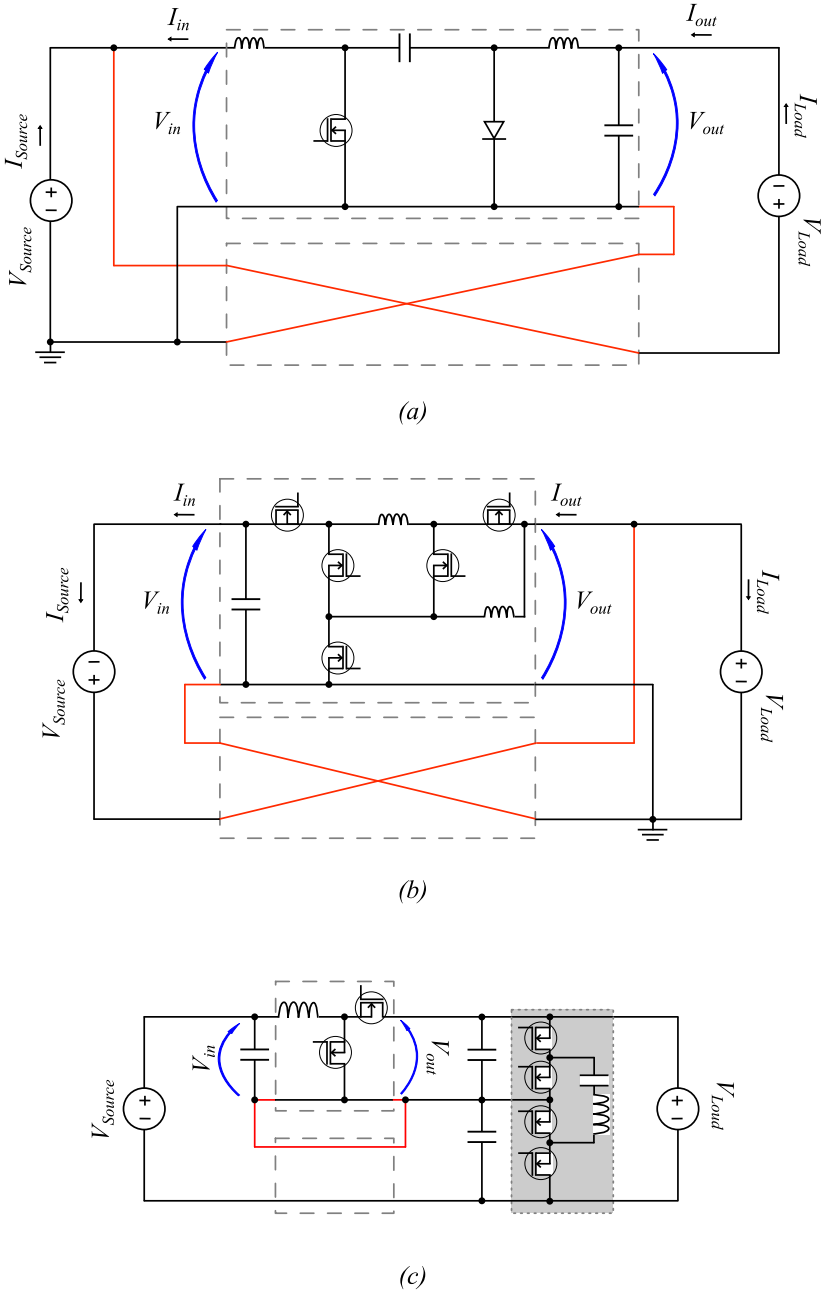

Figure 15. Examples of non-isolated PPC: (**a**) Cuk converter FPC demostrated in [47]. (**b**) Modified Inductor FPC topology seen in [6,46]. (**c**) Boost FPC studied by [43]; shaded area represents *Active Voltage Balancer*.

Second of all, due to the introduction of the Active Voltage Balancer in the design, a straightforward comparison is no longer valid with other topologies as the extra losses and the component count of the balancer have to be accounted for.

5. Conclusions

This review focuses on partial power processing technology, providing a comprehensive review from three aspects: structural classification, theoretical operation limits, and prototype examples. It discusses the principles of partial power processing technology, summarizes and clarifies the classification and naming of partial power structures in existing research, revisits the component stress factors and non-active power factor, and provides certain guidance for researching partial power DC converters.

Compared with traditional full-power solutions, partial power DC converters can achieve direct transmission of main power, with only a small portion of the system's power being processed internally with a DC-DC converter, resulting in performance improvements in cost, volume, power density, efficiency, and thermal design. However due to the specific nature of its circuit structure, there are certain limitations in its application scenarios, and the applicability of partial power solutions needs to be considered in combination with specific scenario characteristics.

Existing research has essentially validated the energy efficiency advantages of PPC compared to traditional full-power converters. This work intends to contribute on the entry and foundation levels to the field of partial power conversion and act as a reference and base for further future development. In the future, further research can be conducted from the following two perspectives: In terms of research content, fault tolerance and fault detection techniques can be of interest as can exploring configurations based on *resonant* converters. Research and optimization for partial power solutions can be performed in *multi-domain* environments, such as *vehicle-to-grid* applications, green hydrogen production, kinetic energy recovery and regeneration for electric mobility, power supply for new data centers, hybrid energy storage systems, energy routers, etc.

Author Contributions: Conceptualization, R.G. and O.G.; methodology, R.G.; analysis, R.G. and R.R.; investigation, O.G.; writing—original draft preparation, O.G. and R.R.; writing—review and editing, R.G., O.G. and A.B.; visualization, O.G.; supervision, R.G. and A.B. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported by grant MCINN-22-TED2021-129796B-C21 and MCINN-23-PID2022-139479OB-C22 funded by MCIN/AEI /10.13039/501100011033. This work has been partially funded from the EUH2020 R&I Program under grant agreement 864459 (Project "TALENT") and through ERFD Structural Funds. This work has been partially supported by PID2019-111051RB-100 (Project "B2B- Energy").

Data Availability Statement: Not applicable.

Conflicts of Interest: The authors declare no conflict of interest.

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