An Insight into the Switching Process of Power MOSFETs: An Improved Analytical Losses Model

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Abstract—The piecewise linear model has traditionally been used to calculate switching losses in switching mode power supplies due to its simplicity and good performance. However, the use of the latest low voltage power MOSFET generations and the continuously increasing range of switching frequencies have made it necessary to review this model to account for the parasitic inductances that it does not include. This paper presents a complete analytical switching loss model for power MOSFETs in low voltage switching converters that includes the most relevant parasitic elements. It clarifies the switching process, providing information about how these parasitics, especially the inductances, determine switching losses and hence the final converter efficiency. The analysis presented in this paper yields two different types of possible switching situations: capacitance-limited switching and inductance-limited switching. This paper shows that, while the piecewise linear model may be applied in the former, the proposed model is more accurate for the latter. Carefully-obtained experimental results, described in detail, support the analytical results presented.

Index Terms—Losses, modeling, MOSFETs, switched mode power supplies.

I. INTRODUCTION

The continuously increasing range of operating frequencies in actual power converters has caused switching losses to greatly determine the final performance of a design. On the one hand, switching losses can be accurately calculated using physical simulation software or circuit simulations that use complete MOSFET models [1]; unfortunately, both methods are quite time consuming, and the information required to obtain precise results is not always available for many designers. Besides, as each simulation only provides valid results for the case under study, neither general conclusions nor a clear physical insight into the switching process are easily obtained from these tools. On the other hand, analytical switching loss models (usually based on certain simplifications) provide less accurate results, but enable the designer to make fast calculations, thus allowing almost immediate comparison between different operating conditions or between different semiconductor performances. Furthermore, analytical models also provide physical insight into the switching process, allowing designers to acquire in-depth knowledge of the switching loss mechanisms.

The classical analytical model, or piecewise-linear model [2], is based on the assumption that MOSFET’s capacitances completely determine its switching behavior. However, it does not account for parasitic inductances. The latest generation of low-voltage power MOSFETs exhibit an extremely good switching performance, mainly due to their low capacitances and increased transconductances; this key fact means that parasitic inductances limit the switching process in practice. The classical model thus needs a review to account for the effect of these parasitics (actual values for the parasitic inductions vary from around 15 nH in a classic TO-220 package to less than 1 n in the DirecFET package used by International Rectifier).

Several detailed models that include such parasitics have already been proposed, including either a fully analytical treatment [3], [4] or a more empirical approach [5]. This issue has also been addressed in [6]–[8], but applied to a current source resonant driver. This paper presents an analytical loss model for power MOSFETs in actual low-medium voltage (< 40 V) switching converters that includes all the parasitics. It is obtained by solving the equivalent circuits during the switching transitions; all the approximations used are clearly stated, and the solutions are presented in a relatively simple form. The model is easy to understand and provides a deep insight into the switching process. The paper is organized as follows: first, the motivation and basis of the model are given. Then, the model and the procedure employed to obtain all the waveforms are fully explained. Finally, the proposed model is compared to the classical model and tested by means of several experiments.

II. MOTIVATION AND BASIS OF THE MODEL

Fig. 1(a) shows a synchronous buck converter. During switching transitions, the output inductance \( L \) may be considered to be a current source, and the output capacitor \( C \) may be considered a constant voltage source. Such assumptions yield the circuit in Fig. 1(b), from which the output voltage has been removed as it is in series with a current source. As the dead time control used in synchronous buck converters causes the freewheeling diode \( D_f \) either to be conducting before the high-side MOSFET, HS, turns on or to start conducting after HS turns off, the low-side MOSFET, LS, does not play any role during the switching transitions, and it can be removed from the circuit. Furthermore, the said dead time forces LS to switch in zero voltage conditions, thus adding no extra losses. Thus, only HS has to be considered in the switching loss analysis. After taking into account such considerations and adding the parasitic capacitances of HS, the
circuit in Fig. 1(c) is obtained. Finally, a rearrangement of the elements in Fig. 1(c) yields the circuit in Fig. 1(d). The same transformations can easily be applied to boost or buck–boost converters, yielding exactly the same final equivalent circuit; the only difference is that the values of voltages and currents change (e.g., in the boost converter the voltage source value is $V_{\text{out}}$ and the current source value is $I_{\text{in}}$). A synchronous buck converter will be used in the following sections to present the model. The major advantage of this approach arises from a practical issue: in a conventional buck converter, conduction losses would mask switching losses due to the high-conduction losses caused by the freewheeling diode $D_f$, thus hindering any laboratory measurement aimed at testing the proposed model. However, it is worth to comment that the analysis is still directly applicable to a conventional buck converter: the only special concern should be that the model would become more difficult to verify due to the aforementioned issues.

A. Range of Application of the Classical Model

The classical model has been widely used by power supply designers. It provides quite accurate results, especially bearing in mind its simplicity. It also provides a simple, comprehensive approach to the switching process. However, careful analysis of the model shows that it is based on the assumption that the switching transitions are strongly determined by the parasitic capacitances. Fig. 2(a) shows the typical turn-ON waveforms in the piecewise-linear model. First, the drain current increases linearly until reaching its final value $I_{\text{out}}$; then, the drain-source voltage drops to 0 V. The procedure is easy to understand: as the freewheeling diode of Fig. 1(d) is initially forward biased, it forces the drain-source voltage to remain constant until the MOSFET carries all the output current. The turn-OFF process is very similar, but the voltage increase takes place before the current. In this situation, the assumptions of the classical model are no longer valid.

B. Basis of the Proposed Model

The proposed model includes the most relevant parasitics present in actual power MOSFETs. Fig. 3(a) shows a simplified physical view of a MOSFET. Three intrinsic parasitic capacitances are considered in this model: the gate-source capacitance, the gate-drain capacitance, and the drain-source capacitance. As both the drain-source capacitance and the gate-drain capacitance are associated with a reverse-biased p-n junction, they change with the applied voltage. This change is modeled by the following equation:

$$C(v) = \frac{C_0}{1 + \frac{v}{K}} \quad (1)$$
beginning of each substage, the equivalent circuit with its corresponding initial conditions is stated. Capacitance values are chosen using (1) in accordance with the initial voltage over the capacitance at the beginning of the substage; though this procedure might yield discontinuities at the substage boundaries, it will provide more accurate results when calculating switching losses and the obtained waveforms will also be more meaningful from a physical point of view. The time-domain equations of the equivalent circuit are then obtained and solved using Laplace transforms. Once the drain current and the internal drain-source voltage are known, switching losses are calculated in terms of energy by integrating the product of those waveforms, and then the energy is multiplied by the switching frequency $f_{sw}$. In certain substages, it is possible to obtain equations that allow the energy losses to be directly found (without an integration procedure). Tables I and II summarize all the relevant equations.

As the final conditions of one substage are used as the initial conditions for the following, and to simplify the use of Laplace transforms, the state variables are chosen such that their initial condition is zero in each substage. Mathematically, $x'(t = 0) = 0$. The initial conditions are included in the circuits and in the corresponding equations as independent voltage sources (for the capacitances) or current sources (for the inductances), but are not drawn in most of the equivalent circuits for the sake of clarity. The actual voltages and currents in the circuits (electrical variables) are noted with an apostrophe, while the state variables are noted without the apostrophe. It is straightforward to find one from the other

$$x'(t) = x(t) + x'(0).$$  

Furthermore, the initial time is chosen as zero at the beginning of each substage.

The ultimate goal of this paper is to obtain relatively simple and handy analytical expressions of voltage and current waveforms that enable the designer to easily calculate switching losses using a conventional spreadsheet. A simple model for MOSFET behavior must be used to achieve such objective. Thus, the MOSFET is considered to be a resistance, an open switch, and a current source in all the analytical calculations presented in this paper. The behavior as a dependent current source (controlled by the voltage between $S_{int}$ and $G_{int}$) is described by (3).

$$i_{channel} = g_m (v_{gs} - V_{TH})$$  

$g_m$ and $V_{TH}$ being the MOSFET transconductance and the threshold voltage, respectively. Obviously, modeling MOSFET behavior using (3) provides results with limited accuracy. However, its use provides a physical insight into the switching process that would be very difficult to obtain if more complicated expressions were used.

### III. Turn-on Transition

The equivalent circuit at the beginning of the turn-on transition is shown in Fig. 6. As the freewheeling diode is forward biased, the voltage $V_{in}$ is applied over the MOSFET equivalent circuit and its parasitics. A detailed analysis of this circuit leads to the four different substages described in the following sections.
TABLE I
SUMMARY OF LOSS CALCULATIONS DURING TURN-ON

Substage I: Duration: \( t_1 \Rightarrow v_{gs} (t_1) = V_{TH} \)

\[
v_{gs} (t) = V_g \cdot \left[ 1 - \frac{1}{\omega_0} \left( \xi^2 - 1 \right)^{-\xi t - \omega_0} \left( \omega_0 \sqrt{\xi^2 - 1} \right) \cosh \left( \omega_0 \sqrt{\xi^2 - 1} t \right) + \xi \omega_0 \sqrt{\xi^2 - 1} \sinh \left( \omega_0 \sqrt{\xi^2 - 1} t \right) \right]
\]
\[
i_g = e^{-t - \xi \omega_0} \sinh \left( \frac{\omega_0 \sqrt{\xi^2 - 1}}{\xi - 1} \right) \cdot C_{eq} \cdot V_g
\]
\[
\omega_0 = \frac{1}{\sqrt{L_{eq} C_{eq}}} , \xi = \frac{L_{eq} L_{gs} L_{gd}}{L_{eq} \left( L_{gs} + L_{gd} \right)} , \ L_{eq} = L_g + \frac{L_{gd} L_{ds}}{L_{gd} + L_{ds}} , \ C_{eq} = C_{gs} + C_{gd}
\]
Power loss \( \Rightarrow P_1 = 0 \)

Substage II: Duration: \( t_2 \Rightarrow v_{ds} (t_2) = -V_{in} \)

\[
v_{gs} (t) = K_1 \left[ \frac{1}{2} \left( -\omega_0 \left( \xi^2 - 1 \right)^{-\xi t - \omega_0} \left( \omega_0 \sqrt{\xi^2 - 1} \right) \cosh \left( \omega_0 \sqrt{\xi^2 - 1} t \right) + \omega_0 \sqrt{\xi^2 - 1} \left( -\xi + \alpha \omega_0 \right) \sinh \left( \omega_0 \sqrt{\xi^2 - 1} t \right) \right) \right]
\]
\[
v_{ds} (t) = K_1 \frac{g_m}{C_{gd} + C_{ds}} \left[ \sinh \left( \frac{t \omega_0 \sqrt{\xi^2 - 1}}{\omega_0 \sqrt{\xi^2 - 1}} \right) e^{-t - \xi \omega_0} \right] \frac{\omega_0 \left( \alpha - \beta \right) - 2 \xi^2 + \alpha \beta \omega_0^2 + 1}{\omega_0^3}
\]
\[
\omega_0 = \sqrt{\frac{M}{L_{eq} C_{eq}}} , \xi = \frac{1}{2} \left( \frac{R_g}{\sqrt{L_{eq} M}} + \frac{1}{R_g} \sqrt{\frac{M \left( M - 1 \right)}{M C_{eq,2}}} \right) , \ K_1 = \frac{g_m}{M} \left( V_g - V_{th} \right) , \ \beta = \frac{C_{gd}}{g_m} , \ \alpha = \frac{I_{g,1} L_{eq}}{V_g - V_{th}}
\]
\[
L_{eq} = L_g + L_s , \ C_{eq} = C_{gs} + \frac{C_{gd} C_{ds}}{C_{gd} + C_{ds}} , \ M = 1 + R_g g_m \frac{C_{gd}}{C_{gd} + C_{ds}}
\]
Power loss \( \Rightarrow P_2 = \int_0^{t_2} g_m v_{gs} (t) (v_{ds} (t) + V_{in}) \, dt \)

Substage III: Duration: \( t_3 \Rightarrow i_d (t_3) = I_{out} \)

\[
i_d = i_d' \approx \frac{V_{in}}{L_{ds} + L_s} t
\]
Power loss \( \Rightarrow P_3 \approx 0 \)

Substage IV: reverse recovery period
Power loss \( \Rightarrow P_4 = \left( V_{in} Q_{rr} - \frac{1}{2} C_D V_{in}^2 \right) f_{sw} \)

A. Substage I
During substage I, the gate-source equivalent capacitance is charged until it reaches \( V_{TH} \). As the MOSFET is open circuited, approximately no drain current flows in the circuit and the drain-source voltage remains constant. Thus, only the gate circuit must be considered. The equivalent circuit is shown in Fig. 7. The initial conditions for the electrical variables are:
\[
i_g' (0) = 0 \quad (10)
\]
\[
v_{gs}' (0) = 0 .
\]
From the circuit in Fig. 7, the following equations are obtained:
\[
V_g = \left( L_g + \frac{L_s L_{gd}}{L_{ds} + L_s} \right) \frac{d i_g}{dt} + i_g R_g + v_{gs}
\]
\[
i_g = (C_{gs} + C_{gd}) \frac{d v_{gs}}{dt}.
\]
Applying Laplace transforms to (12) and (13) and solving for \( v_{gs} \) yields
\[
v_{gs} (s) = \frac{1}{s L_{eq} C_{eq} s^2 + R_g C_{eq} s + 1} \]
\[
L_{eq} \text{ and } C_{eq} \text{ now being}
\]
\[
L_{eq} = \left( L_g + \frac{L_s L_{gd}}{L_{ds} + L_s} \right) , \ \ C_{eq} = (C_{gs} + C_{gd}) .
\]
The inverse Laplace transform of (14) is shown in Table I as (4). The current \( i_g \) can be obtained from (12) and (13), following the same procedure. This current, as shown in Table I as (5), is used to calculate the initial current for the following substage. As the MOSFET is not activated, there is no power loss during this period, except for the losses in the gate drive circuit that are included as a separate term in the final loss calculations.
TABLE II
SUMMARY OF LOSS CALCULATIONS DURING TURN-OFF

Substage I: Duration: \( t_1 \rightarrow v_{gs}(t_1) = -V_g + V_{TH} + \frac{I_{out}}{g_m} \)

\[
v_{gs}(t) = -V_g + \frac{1}{\omega_0(\xi^2 - 1)} e^{-t \xi} \left( \omega_0 \sqrt{\xi^2 - 1} \cosh \left( \omega_0 \sqrt{\xi^2 - 1} t \right) + \xi \omega_0 \sqrt{\xi^2 - 1} \sinh \left( \omega_0 \sqrt{\xi^2 - 1} t \right) \right)
\]

\[
i_g = -e^{-t \xi} \omega_0 \sinh \left( \omega_0 \sqrt{\xi^2 - 1} \right) \cdot \frac{\omega_0(\xi^2 - 1)}{(\xi^2 - 1)} \cdot C_{eq} \cdot V_g
\]

\[
\omega_0 = \frac{1}{L_{eq}C_{eq}}, \xi = \frac{R_g}{2} \sqrt{\frac{C_{eq}}{L_{eq}}}, L_{eq} = L_g + L_d, C_{eq} = C_{gs} + C_{gd}
\]

Power loss \( \Rightarrow P_1 = 0 \)

Substage II: Duration: \( t_2 \rightarrow v_{ds}(t_2) = V_{in} \)

\[
v_{gs}(t) = K_1 \left[ -\frac{1}{\omega_0^2} + \frac{e^{-t \xi \omega_0}}{\omega_0^2(\xi^2 - 1)} \left( \omega_0 \sqrt{\xi^2 - 1} \cosh \left( t \omega_0 \sqrt{\xi^2 - 1} \right) + \omega_0 \sqrt{\xi^2 - 1} \left( \xi - \alpha \omega_0 \right) \sinh \left( t \omega_0 \sqrt{\xi^2 - 1} \right) \right) \right]
\]

\[
v_{ds}(t) = K_1 \frac{g_m}{C_{gd} + C_{ds}} \left[ \frac{\left( \xi \omega_0 - \xi \omega_0 \beta - 2 \xi^2 + \alpha \beta \omega_0^2 + 1 \right) \sinh \left( t \omega_0 \sqrt{\xi^2 - 1} \right) e^{-t \xi \omega_0}}{\omega_0^2 \sqrt{\xi^2 - 1}} \right]
\]

\[
\omega_0 = \sqrt{\frac{M}{L_{eq}C_{eq}}}, \xi = \frac{1}{2} \left( \frac{R_g}{\sqrt{\frac{C_{eq}}{L_{eq}}M + \frac{1}{R_g} \sqrt{(M - 1)^2}}}, K_1 = \frac{\omega_0^2}{M} \left( V_{th} + \frac{I_0}{g_m} \right), \beta = \frac{C_{gd}}{g_m}, \alpha = \frac{L_{eq}I_{th,2}}{V_{th} + \frac{I_0}{g_m}} \right)
\]

\[
L_{eq} = L_g + L_d, C_{eq} = C_{gs} + \frac{C_{gd}C_{ds}}{C_{gd} + C_{ds}}, M = 1 + \frac{R_g g_m}{C_{gd} + C_{ds}}
\]

Power loss \( \Rightarrow P_2 = \int_{0}^{t_2} v_{ds}(t) g_m \left( v_{gs}(t) + \frac{I_{out}}{g_m} \right) dt \)

Substage III: Duration \( t_3 \rightarrow I_d(t_3) = I_{ch,\infty} \)

\[
v_{ds}(t) = \left( I_{out} - I_{ch,\infty} \right) L_d \omega_0 \sin \left( \omega_0 t \right)
\]

\[
i_d(t) = - \left( I_{out} - I_{ch,\infty} \right) \left( 1 - \cos \left( \omega_0 t \right) \right)
\]

\[
\omega_0 = \frac{1}{\sqrt{(L_g + L_d)/C_{ds}}}, I_{ch,\infty} = \frac{I_{out} (M - 1) - V_{TH} g_m}{M}
\]

Power loss \( \Rightarrow P_3 = \int_{0}^{t_3} \left( v_{ds}(t) + V_{in} \right) I_{ch,\infty} dt \)

Substage IV: Duration \( t_4 \rightarrow i_{channel}(t_4) = 0 \)

\[
i_{channel}(t) = i_{ch,\infty} - \frac{V_{peak} - V_{in}}{L_s + L_d} t
\]

\[
V_{ds} = V_{ds,peak}
\]

Power loss \( \Rightarrow P_4 = V_{ds,peak} \int_{0}^{t_4} i_{channel}(t) dt \)

Substage V: Power loss \( \Rightarrow P_4 = fsw \left( \frac{1}{2} C_{ds} \left( V_{peak}^2 + V_{in}^2 \right) - C_{ds} V_{peak} V_{in} \right) \)
Fig. 6. Equivalent circuit at the beginning of the turn-ON transition.

Fig. 7. Equivalent circuit during substage I.

Fig. 8. Equivalent circuit during substage II.

B. Substage II

When $v_{gs}$ reaches $V_{TH}$, the MOSFET channel starts conducting. Equation (3) then applies, and the channel current is directly proportional to $V_{gs} - V_{TH}$. Fig. 8 shows the equivalent circuit for this substage.

The initial conditions are:

$$v'_{gs}(0) = V_{TH}$$
$$v'_{gd}(0) = V_{in} - V_{TH}$$
$$v'_{ds}(0) = V_{in}$$
$$i'_{d}(0) = 0$$
$$i'_{g}(0) = i'_{s}(0) = I_{g-1}$$

with $I_{g-1}$ being the initial current in the gate circuit.

A total of seven differential equations can be obtained from the circuit in Fig. 8, one for each state variable in the circuit (yielding six equations) and (3) being the seventh. This set of differential equations can be reduced to four by eliminating three state variables: the current through the source inductance $i_{s}$, the channel current $i_{channel}$, and the voltage across the gate-drain capacitance $v_{dg}$. The remaining set of equations is

$$V_{g} - V_{th} = (i_{g} + I_{g-1}) R_{g}$$
$$+ L_{g} \frac{di_{g}}{dt} + v_{gs} + L_{s} \left( \frac{di_{d}}{dt} + \frac{di_{g}}{dt} \right)$$

$$0 = v_{ds} + L_{d} \frac{di_{d}}{dt} + L_{s} \left( \frac{di_{d}}{dt} + \frac{di_{g}}{dt} \right)$$

$$C_{gs} \frac{dv_{gs}}{dt} = i_{g} + I_{g-1} + C_{gd} \left( \frac{dv_{ds}}{dt} - \frac{dv_{gs}}{dt} \right)$$

$$i_{d} = C_{gd} \left( \frac{dv_{ds}}{dt} - \frac{dv_{gs}}{dt} \right) + C_{ds} \frac{dv_{ds}}{dt} + g_{m} v_{gs}.$$  

As this set of equations is, in general, coupled, a simple analytical solution cannot be easily found. However, considering the typical values of the capacitances and transconductances in modern low-voltage power MOSFETs, it can be concluded that the channel current will increase very fast, rapidly discharging the drain-source capacitance. The parasitic inductances stop the drain current from increasing, thus allowing $C_{ds}$ to be discharged by the channel current. The drain current $i_{d}$ and its derivatives can be neglected.

Equation (34) is no longer needed, and the other three equations are uncoupled. Thus, the remaining set of equations can be solved to find voltages and currents in a simple form. Using Laplace transforms, $v_{gs}(s)$ is obtained as

$$v_{gs}(s) = \frac{1}{s} \left( \frac{V_{g} - V_{th} + I_{g-1} L_{eq} s}{s^2 (L_{eq} C_{eq}) + s (R_{g} C_{eq} + (M - 1) (L_{eq}/R_{g})) + M} \right)$$
Fig. 9. Equivalent circuit during substage III.

with \( M, L_{eq} \) and \( C_{eq} \) now being

\[
M = 1 + R_g g_m \frac{C_{gd}}{C_{gd} + C_{ds}}
\]

\[
L_{eq} = L_g + L_s \quad C_{eq} = C_{gs} + \frac{C_{gd} C_{ds}}{C_{gd} + C_{ds}}.
\]

The inverse Laplace transform of (37) is shown in Table I as (6). The drain-source voltage state variable can also be obtained by applying Laplace transforms to \( v_{ds} \).

\[
v_{ds}(s) = \frac{g_m}{s^2 (C_{gd} + C_{ds})} \left( V_g - V_{th} + I_{g,1} L_{eq} s (s (C_{gd} / g_m) - 1) + s (R_g C_{eq} + (M - 1) (L_{eq} / R_g)) + M \right).
\]

The inverse Laplace transform of (38) is shown in Table I as (7). The power loss during this substage has to be found by integrating the product \( i_{channel} v_{ds} \). The end of this substage takes place when the drain-source voltage reaches approximately 0 V.

If the input voltage were higher than a few tens of volts, \( V_{ds} \) would not reach 0 V, but would tend to reach an intermediate voltage. As the present analysis is limited to input voltages below approximately 40 V, this situation is not considered and \( V_{ds} \) will drop to 0 V in most practical situations.

C. Substage III

After the drain-source voltage reaches approximately 0 V, the MOSFET starts behaving as a resistor. Fig. 9 shows the equivalent circuit. The initial condition is

\[
i_d'(0) \approx 0.
\]

Thus, the drain current is approximately determined by the input voltage source and the parasitic inductances

\[
i_d' \approx \frac{V_{in}}{L_d + L_s} t.
\]

Once again, the state variable \( i_d' \) and the actual drain current \( i_d' \) are the same. As this substage lasts for a short period of time and \( R_{ds,ON} \) is usually very low, switching losses can be neglected. This substage finishes when the drain current reaches the output current.

D. Substage IV

This substage, which is usually called the reverse recovery period, has been extensively analyzed in [3]. When the drain current reaches the output current, the reverse recovery period begins. Fig. 10(a) shows the equivalent circuit at the beginning of this period. The freewheeling diode is unable to block reverse voltage until a certain amount of charge has been removed from its junction. Thus, the drain current increases until it reaches a certain peak current \( I_{peak} \); at this moment, the charge has been removed from the diode junction and it becomes capable of blocking reverse voltage. Fig. 10(c) shows the equivalent circuit at this moment, \( C_D \) being the equivalent freewheeling diode capacitance. A resonant period then begins, at the end of which the capacitance is charged to \( V_{in} \) and the current through the inductance is \( I_{out} \) once again.

Fig. 11 shows the definition of the reverse recovery charge \( Q_{rr} \) and the reverse recovery time \( t_{rr} \), under common test conditions. The reverse recovery charge is the total charge that has to be provided to the diode junction until the voltage across it reaches its steady-state value and the current through the diode drops to 0 A. The charge provided to the equivalent diode capacitance during the resonant period is hence included in the term \( Q_{rr} \). This is the major difference between the present analysis and previously presented results.

The energy stored in the circuit at the beginning of substage IV is

\[
E_L = \frac{1}{2} \left( L_s + L_d \right) I_{out}^2
\]

\[
E_{C_D} = 0.
\]
When the current reaches \( I_{\text{peak}} \), the energy stored in the inductance is

\[
E_{L, \text{peak}} = \frac{1}{2} (L_s + L_d) I_{\text{peak}}^2.
\] (43)

The energy provided by the voltage source during said period is

\[
E_{V_{\text{in}}} = V_{\text{in}} Q_{rr, 1}
\] (44)

with \( Q_{rr, 1} \) being the part of \( Q_{rr} \) that is removed from the diode before the current reaches \( I_{\text{peak}} \). Thus, the energy loss is

\[
E_{\text{loss, 1}} = V_{\text{in}} Q_{rr, 1} - \frac{1}{2} (L_s + L_d) \left( I_{\text{peak}}^2 - I_{\text{out}}^2 \right).
\] (45)

During the resonant period, the energy stored in the inductance changes from \( \frac{1}{2} (L_s + L_d) I_{\text{peak}}^2 \) to \( \frac{1}{2} (L_s + L_d) I_{\text{out}}^2 \), so the net energy provided to the inductance during the whole substage is zero. The energy loss during the resonant period is

\[
E_{\text{loss, 2}} = V_{\text{in}} Q_{rr, 2} - \frac{1}{2} C_D V_{\text{in}}^2 + \frac{1}{2} (L_s + L_d) \left( I_{\text{peak}}^2 - I_{\text{out}}^2 \right)
\] (46)

with \( Q_{rr, 2} \) being the part of \( Q_{rr} \) that is needed to charge the equivalent parasitic diode capacitance once it is able to block reverse voltage. The second term in (46) stands for the final energy stored in the diode parasitic capacitance. The total energy loss is thus given by (47)

\[
E_{\text{loss}} = E_{\text{loss, 1}} + E_{\text{loss, 2}} = V_{\text{in}} \left( Q_{rr, 1} + Q_{rr, 2} \right) - \frac{1}{2} C_D V_{\text{in}}^2
\] (47)

As \( C_D \) depends on the applied voltage, (47) can be rewritten as

\[
E_{\text{loss}} = V_{\text{in}} Q_{rr} - \frac{1}{2} Q_D V_{\text{in}}
\] (48)

with \( Q_D \) being the total charge supplied to the diode junction; this charge can be calculated integrating the capacitance versus voltage graph.

Noteworthily, significant reverse recovery parameters are very difficult to calculate; for instance, \( Q_{rr} \) strongly depends on \( I_{\text{out}} \) and on the rate of change of the current, see, e.g., [10]. If the freewheeling diode is a Schottky diode, which suffers almost no reverse recovery effects, then (47) becomes

\[
E_{\text{loss}} = V_{\text{in}} \left( \frac{Q_{rr}}{V_{\text{in}} C_{\text{Schottky}}} \right) - \frac{1}{2} C_{\text{Schottky}} V_{\text{in}}^2 = \frac{1}{2} C_{\text{Schottky}} V_{\text{in}}^2
\] (49)

with \( C_{\text{Schottky}} \) being the Schottky diode equivalent capacitance.

### E. Example Waveforms

Fig. 12 shows a set of example waveforms provided by the model, using typical MOSFET parameters. Fig. 12(a) shows the drain to source voltage and the channel current, as well as the instantaneous power in the channel, during the first three substages (the reverse recovery substage has not been included). It can be seen that, as long as the reverse recovery process is not taken into account, significant power loss only takes place during substage II, which lasts for a relatively short period. Thus, the model suggests that, when an inductance-limited switching takes place, there are small turn-on losses. Furthermore, as stated in [11], there is no need to include the rather arbitrary output capacitance loss term, \( \frac{1}{2} C_{D_{\text{out}}} V_{\text{in}}^2 \). Fig. 12(b) shows the gate to source voltage; it can be seen that the Miller effect takes place during substage II, and that it is predicted by the analytical model. The gate to source voltage is essentially equal to that of the classical model and to the waveforms found in conventional MOSFET datasheet.

### IV. TURN-OFF TRANSITION

The equivalent circuit at the beginning of the turn-off transition is shown in Fig. 13. As the freewheeling diode is reverse biased, the current \( I_{\text{out}} \) circulates through the MOSFET and the parasitic inductances. A detailed analysis of this circuit leads to the five different substages described in the following sections.

#### A. Substage I

The gate circuit discharges the gate-source equivalent capacitance. Fig. 14 shows the equivalent circuit during this period. The initial conditions are

\[
v'_{g_{s}}(0) = V_{g}
\] (50)

\[
v_{g}(0) = 0.
\] (51)
Fig. 12. (a) Turn-ON example waveform (the reverse recovery period is not included). The sudden change in the channel current is a consequence of the approximations that were made during the analysis; (b) gate to source voltage example waveform. The Miller effect takes place during substage II and causes the actual channel current waveform.

Fig. 13. Equivalent circuit at the beginning of the turn-OFF transition.

From the circuit in Fig. 14, the following equations can be easily obtained:

\[-V_g = (L_g + L_s) \frac{d i_g}{d t} + i_g R_g + v_{gs}\]  \hspace{1cm} (52)

\[i_g = (C_{gs} + C_{gd}) \frac{dv_{gs}}{dt}.\]  \hspace{1cm} (53)

Using Laplace transforms, \(v_{gs}\) is found

\[v_{gs}(s) = \frac{V_g}{s L_{eq} C_{eq} s^2 + R_g C_{eq} s + 1}\]  \hspace{1cm} (54)

\(L_{eq}\) and \(C_{eq}\) now being

\[L_{eq} = L_g + L_s \quad C_{eq} = C_{gs} + C_{gd}.\]

The inverse Laplace transform of (54) is shown in Table II as (15). The current \(i_g\) can be obtained from (52) and (53), following the same procedure. This current, as shown in Table II as (16), is used to calculate the initial current for the following substage. Even though the MOSFET is carrying the output current, this period lasts for a short time and the losses can be neglected.

Substage I finishes at a time \(t_1\), when the MOSFET enters into the linear region, where (3) applies. Thus, \(t_1\) can be calculated as

\[v_{gs}(t_1) = -V_g + V_{TH} + \frac{I_{out}}{g_m}.\]  \hspace{1cm} (55)

B. Substage II

Fig. 15 shows the equivalent circuit during this period. The channel current suddenly decreases, thus causing the excess current \(I_{out} - i_{channel}\) charging the MOSFET capacitances. The initial conditions are

\[v'_{gs}(0) = V_{TH} + \frac{I_{out}}{g_m}\]  \hspace{1cm} (56)

\[v'_{ds}(0) = -\left( V_{TH} + \frac{I_{out}}{g_m} \right)\]  \hspace{1cm} (57)

\[v'_{ds}(0) \approx 0\]  \hspace{1cm} (58)

\[i'_g(0) = -I_{g,2} \]  \hspace{1cm} (59)

\[i'_d(0) = I_{out}\]  \hspace{1cm} (60)

\[i'_s(0) = I_{out} - I_{g,2}\]  \hspace{1cm} (61)

with \(I_{g,2}\) being the initial current in the gate circuit.
The circuit equations are the following:

\[ 0 = \left( i_g + I_{g,2} \right) R_g + L_g \frac{di_g}{dt} - v_{gs} - \left( V_{TH} + \frac{I_{out}}{g_m} \right) + L_s \frac{di_s}{dt} \tag{62} \]

\[ v_{ds} = v_{gs} + v_{gd} \tag{63} \]

\[ i_g + I_{g,2} + C_{gs} \frac{dv_{gs}}{dt} = C_{gd} \frac{dv_{gd}}{dt} \tag{64} \]

\[ I_{out} - C_{ds} \frac{dv_{ds}}{dt} = i_{channel} + C_{gd} \frac{dv_{gd}}{dt} \tag{65} \]

\[ i_g + i_s = 0 \tag{66} \]

These equations can be solved directly using Laplace transforms to find \( v_{gs} \)

\[ v_{gs}(s) = -\frac{1}{s} \frac{s L_{eq} I_{g,2} + (V_{TH} + (I_{out}/g_m))}{L_{eq} C_{eq} s^2 + (R_g C_{eq} + (M - 1) (L_{eq}/R_g)) s + M} \tag{67} \]

with \( M, L_{eq}, \) and \( C_{eq} \) being the same as in Section III-B

\[ L_{eq} = L_s + L_g \quad C_{eq} = C_{gs} + \frac{C_{ds} C_{gd}}{C_{gd} + C_{ds}} \]

\[ M = 1 + R_g g_m \frac{C_{gd}}{C_{gd} + C_{ds}} \]

Applying the inverse Laplace transform to (67) yields (17) in Table II. The results are very similar to those obtained in Section III-B. The drain-source voltage can be obtained from (62)–(66) using the same procedure. The result is shown in Table II as (18). This period ends when the drain-source voltage reaches \( V_{in} \). The channel current could reach 0 A before that moment; such a situation will be addressed in Section IV-F.

### C. Substage III

At the beginning of this substage, \( v'_{ds} \) has reached \( V_{in} \) and the freewheeling diode becomes forward biased. Fig. 16(a) shows the equivalent circuit during this period. The initial conditions are

\[ i_d(0) = I_{out} \tag{68} \]

\[ v'(0) \approx I_{out} \tag{69} \]

\[ i_{channel}(0) = I_{ch,\infty} \tag{70} \]

\[ v'_d(0) = V_{in} \tag{71} \]

As the drain inductance impedes a sudden change in the drain current, the drain-source voltage continues increasing. It is assumed that the gate voltage remains constant during this period, and as does the channel current. The latter can be approximated

\[ I_{ch,\infty} = \lim_{t \to \infty} i_{channel} = \lim_{s \to 0} g_m V_{gs}(t) \]

\[ = \frac{\lim_{s \to 0} s v_{gs} + V_{TH} + \frac{I_{out}}{g_m}}{M} \tag{72} \]

In this substage, the initial conditions have been represented by independent voltage and current sources in the circuit in Fig. 16(a); instead of solving the circuit equations, a rearrangement of these sources easily yields the circuit in Fig. 16(c).

Fig. 16(c) shows that the final equivalent circuit is a simple parallel resonant circuit. As the current and voltage waveforms in this circuit are oscillating, it seems clear that the proposed approximation is valid as long as the substage lasts for a time shorter than half a resonant period. \( v_{ds} \) is easily found from Fig. 16(c)

\[ v'_{ds}(t) = V_{in} + (I_{out} - I_{ch,\infty}) L_d \frac{\omega_0}{2} \sin(\omega_0 t) \tag{73} \]

with \( \omega_0 \) being

\[ \omega_0 = \frac{1}{\sqrt{(L_s + L_d) C_{ds}}} \tag{74} \]

This substage ends when the drain current reaches the channel current \( I_{ch,\infty} \). At this moment, the drain-source voltage has reached its peak voltage \( V_{ds,peak} \). This value can easily be calculated once \( t_3 \) is known.

\[ V_{ds,peak} = v'_{ds}(t_3) \tag{75} \]

### D. Substage IV

During this period, the drain current continues decreasing toward zero, forced by the voltage difference that exists between
$C_{ds}$ is considered to remain approximately equal to $V_{ds,peak}$ during this period. Thus, $V_{ds}$ is considered to remain approximately equal to $V_{ds,peak}$ during this substage. In order to simplify the analysis, the channel current is assumed to decrease as if it were controlled by the voltage source $V_{in}$ instead of by the gate-source voltage. The power loss can thus be obtained as

$$P_{loss} = \int V_{ds}i_{channel}dt \approx V_{ds,peak} \int i_{channel}dt.$$  \hspace{1cm} (76)

Fig. 17(a) shows the equivalent circuit. Thus, the channel current can be approximated as

$$i_{channel}(t) = I_{ch,\infty} - \frac{V_{ds,peak} - V_{in}}{L_s + L_d} t.$$  \hspace{1cm} (77)

### E. Substage V

A resonant stage begins when the channel current reaches 0 A; the MOSFET stops conducting current and becomes an open circuit. The gate circuit continues discharging $C_{gs}$ and $C_{gd}$ more or less independently from the rest of the circuit. At the same time, the resonant circuit formed by $L_s + L_d$ and $C_{ds}$ starts oscillating until it reaches its steady-state value. The equivalent resistance is shown in Fig. 17(b). $R$ stands for the equivalent resistance that dumps the oscillations, which is mainly made up of the circuit tracks high-frequency resistance and the parasitic inductance and capacitance high-frequency equivalent resistances.

The loss calculations during this substage are identical to those in Section III-D. Once again, losses can be calculated by considering the energy stored at the beginning and the end of the substage. The energy stored at the beginning is

$$E_L = 0$$  \hspace{1cm} (78)

$$E_{C,i} = \frac{1}{2} C_{ds} (V_{ds,peak})^2.$$  \hspace{1cm} (79)

The energy stored at the end of the period is

$$E_L = 0$$  \hspace{1cm} (80)

$$E_{C,f} = \frac{1}{2} C_{ds} V_{in}^2.$$  \hspace{1cm} (81)

### F. Example Waveforms

Fig. 18 shows a set of example waveforms provided by the model, using typical MOSFET parameters. As the gate to source voltage provided by the model is again essentially equal to what can be found in a conventional MOSFET datasheet, it has not been included in this section. It can be seen in Fig. 18 that a noticeable power loss occurs during the turn-off transition, especially in comparison with the turn-on. Thus, the model suggests that turn-off switching losses are much higher than turn-on switching losses.

This fact can be easily explained taking into consideration the effect of the parasitic inductances: these limit the current

The energy provided by the voltage source is

$$E_{V_{in}} = V_{in}C_{ds} (V_{in} - V_{ds,peak})$$  \hspace{1cm} (82)

an equation that shows that some energy has been returned to the input source. Finally, the energy loss is

$$E_{loss} = E_{V_{in}} - (E_{C,i} - E_{C,f})$$

$$= \frac{1}{2} C_{ds} (V_{peak}^2 + V_{in}^2) - C_{ds} V_{peak} V_{in}.$$  \hspace{1cm} (83)

The latter expression is the same as the one obtained in [3].

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As previously stated in Section IV-B, the channel current could drop to 0 A during substage II, thus causing a sudden end of said substage. This is likely to happen if $I_{out}$ is relatively small. In that case, the MOSFET becomes open circuited and the analysis is straightforward; switching losses during the rest of the turn-off transition can be approximated by considering that all the energy stored in the parasitic inductances is lost during the resonant period

$$E_{loss} \approx \frac{1}{2} (L_s + L_d) I_{out}^2.$$  \hspace{1cm} (84)

Equation (84) neglects the voltage difference between $V_{ds}$ and $V_{in}$ at the moment when this substage begins.

However, as the switching losses given by (84) are noticeably smaller than in the normal switching transition, this case is of minor relevance.

### G. Example Waveforms

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change rate during turn-ON, thus inducing an almost zero-current-switching transition. Conversely, during the turn-OFF transition, the inductances lengthen the duration of the process, thereby causing an increase in the losses.

V. COMPARISON WITH THE CLASSICAL PIECEWISE-LINEAR MODEL

Fig. 19 shows a comparison between the results provided by the classical model (extracted from [2]) and the proposed model. It is apparent that the classical model yields higher losses during turn-ON than the proposed model, whereas during turn-OFF the opposite happens and the classical model yields smaller losses than the proposed model.

However, there is a “compensation effect” between these two errors that leads to the final losses not being very different from one model to another. This coincidence means that the classical model is still very useful, but only when the switching process is not inductance limited: in that case it yields inaccurate results, as is shown in Section VI. The proposed model clearly indicates that turn-OFF losses are much higher than turn-ON losses in the inductance-limited case.

From a designer’s point of view, it is interesting to establish an approximate boundary between the region where the classical model can be reliably applied (capacitance-limited switching) and the region when the proposed model should be used because the effect of parasitic inductances cannot be neglected (inductance-limited switching). The classical model states that the turn-ON time is

\[ t_{\text{turn-on}} = \frac{Q_{\text{switching}} R_d}{V_{th} + (I_{\text{out}}/g_m)} \]  

(85)

with \( Q_{\text{switching}} \) being the total switching charge that has to be transferred into the gate-drain capacitance during the Miller effect period, the value of which is usually given in the datasheet. Thus, the current increase through \( L_d \) during the estimated turn-ON time can be compared with the output current \( I_{\text{out}} \): if the latter is much smaller than the former, \( L_d \) will not be able to limit the current rate of change and the switching will be capacitance limited. On the contrary, if \( I_{\text{out}} \) is much bigger than the current increase through \( L_d \), then \( L_d \) will limit the current rate of change.

\[
I_{\text{out}} << \frac{t_{\text{turn-on}} V_{\text{in}}}{2L_d} \Rightarrow \text{capacitance limited} \tag{86}
\]

\[
I_{\text{out}} >> \frac{t_{\text{turn-on}} V_{\text{in}}}{2L_d} \Rightarrow \text{inductance limited}. \tag{87}
\]

A comprehensive differentiation of these two cases can also be found in [12].

VI. EXPERIMENTAL RESULTS

To experimentally test the proposed model, several laboratory measurements were conducted. First, the efficiency of a synchronous buck converter was measured and compared with the data provided by the proposed model. A National Semiconductor LM3152 demo board switching at 500 kHz (see Fig. 20) was used. As not enough reverse recovery data are given in the datasheet of the MOSFETs (RJK0305), a Schottky diode was connected in parallel with the low-side MOSFET. Thus, (49) can be used to estimate the losses during substage IV of the turn-ON transition. Conduction losses of both MOSFETs and the diode were fully taken into account and calculated using conventional equations (e.g., in the case of one of the MOSFETs, the expression \( t_{\text{in}} R_{ds,ON} \) was used, \( t_{\text{in}} \) being the root mean square current through the MOSFET); power losses in input and output capacitances and in the control circuitry were also considered, as well as the increase of the MOSFETs on-resistance with operating temperature.

The results are shown in Fig. 21(a) and (b). It can be seen that the model provides accurate results and that the trend followed by experimental data is clearly reproduced by the model. Switching losses account for approximately 25% of the total amount of losses in this experiment. There is a certain amount of uncertainty in the efficiency results provided by the model mainly caused by the uncertainty in the current ripple of the demo board output inductance and by the reverse recovery losses that may still be existing in the circuit.

A second experiment was carried out to minimize these uncertainties. A synchronous buck converter switching at 1.3 MHz was built using RJK0305 MOSFETs and an LM2727 controller. Several changes were made with respect to the previously described experiment. First, the switching frequency was increased to give more weight to switching losses against other loss terms. Second, a very small inductor (\( \approx 300 \) nH) was used to obtain a
very high current ripple. The effect of reverse recovery losses was thus diminished, because the inductor current at the turn-ON instant was much smaller than the current at the turn-OFF. Moreover, the high current ripple allowed us to have less average output current while maintaining a high turn-OFF current, thus achieving lower conduction losses and giving more weight to switching losses. As core losses were also another source of uncertainty, a coreless inductor was used. The output voltage ripple was kept small by incrementing the output capacitance \( \approx 150 \mu F \) and by using several low-equivalent series resistance capacitors. Third, the current through the inductor was measured using a current transformer built with a small toroid. Fig. 22 shows the prototype. Switching losses were more than 30% of total losses with this setup.

Two different sets of measurements were made: first, the efficiency was measured and compared to the results provided by the classical model and the proposed model; second, a small drain inductance was added to the circuit and the efficiency was measured again. Fig. 22 shows how the inductance was achieved in practice: the decoupling capacitors were separated about 1 cm from their previous position. The current loop that causes the inductance was thus made longer and the inductance was increased. The layout was measured by a precision impedance analyzer before and after the change. The measurements yielded an extra inductance of approximately 10–15 nH.

Fig. 23 shows a comparison between the experimental results obtained and the results provided by the classical and the proposed model. Fig. 23(a) demonstrates that both the classical and the proposed model can approximately reproduce the measured efficiency when decoupling capacitances are in position 1; i.e., when the parasitic inductance is minimized. An error of nearly one point can be appreciated in the results: as the exact values of most of the parameters are not precisely known, it is very difficult to achieve more accuracy using datasheet values, regardless of the model being used.

Fig. 23(b) shows the results when the decoupling capacitors are in position 2. It is apparent that, as the classical model does
not take into account any inductance, its results were noticeably different from the measured data. In contrast, the proposed model was able to reproduce the experimental efficiency.

Fig. 24 shows the breakdown of losses provided by the proposed and the classical model. These values were used to obtain the results, as shown in Fig. 23. The influence of each contribution can be clearly appreciated: as stated, the contribution of switching losses to the total losses was above 30%. Fig. 25 shows the detailed contribution of each loss term when the average output current was 7 A. Yet again, the contribution of switching losses to the total losses can be clearly noticed, along with the higher contribution of the turn-off term in all operating conditions. Furthermore, the extra drain inductance (the capacitance in position 2) only increased the turn-off losses, while the rest of the terms remained constant.

VII. CONCLUSION

This paper has presented a new detailed switching model for power MOSFETs, which allows switching losses to be calculated. It has been shown that although the classical model is very useful and provides relatively accurate results, it may not precise enough in actual synchronous buck converter designs if their switching process is inductance limited. The proposed model takes into account the major circuit parasitics, especially inductances, providing analytical solutions for the waveforms and enabling the designer to create a simple spreadsheet to estimate switching losses. All the equations required for loss calculations are summarized in Tables I and II. Furthermore, the model provides a clear physical overview of the switching process and shows the effect that the different parasitics of the transistor and the circuit have on this process. For instance, it shows that the turn-on and the turn-off transitions are quite different in nature. This paper has shown, via carefully planned experimental measurements, that the model provides quite accurate results. It has also demonstrated that the classical model, though very useful and accurate, has certain application limits; the proposed model is intended to provide better results than the classical model in such situations. The conditions in which each model should be used have also been stated, clearly differentiating between capacitance-limited switching and inductance-limited switching.

The experimental results have also shown that it is very difficult to accurately predict the efficiency, regardless of the model being used, mainly due to the uncertainty that exists when determining the value of most of the parameters. For instance, both the proposed and the classical model are very sensitive to the MOSFET threshold voltage and the transconductance. As the operating conditions in which these parameters are given in the datasheet may not match actual working conditions, and also given that each parameter has its own variation range within each MOSFET, a certain deviation in the model predictions is almost unavoidable. Furthermore, the values of the parasitic capacitances change with the voltage applied across them, while the parasitic inductances change with the frequency of operation.

It is however worth pointing out that, even though the use of analytical models cannot provide results as accurate as, e.g., a physical simulation software, a relatively precise prediction can be made and tested by carefully planned setups, as this paper has shown.
REFERENCES


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