A Very Simple Control Strategy for Power Factor Correctors Driving High-Brightness LEDs

Diego González Lamar, Member, IEEE, Javier Sebastián Zúñiga, Member, IEEE, Alberto Rodríguez Alonso, Student Member, IEEE, Miguel Rodríguez González, Student Member, IEEE, and Marta María Hernando Álvarez, Member, IEEE

Abstract—This paper presents a new control strategy for power factor correctors (PFCs) that are used to drive high-brightness LEDs. This control strategy is extremely simple and is based on the use of a conventional peak-current-mode controller with a suitable selection of the compensation ramp waveform. Neither an analog multiplier nor an input voltage sensor is needed to achieve quasi-sinusoidal line waveforms at nominal conditions and full load. If the converter belongs to the flyback family (flyback, buck–boost, SEPIC, Cuk and Zeta), the line waveform appears notably distorted if the compensation function is a linear ramp, but becomes almost sinusoidal if the linear ramp is substituted by a properly chosen exponential function. The line waveform is slightly distorted when the load varies or when the converter works under either overvoltage or undervoltage conditions. However, the waveform maintains a very high power factor (PF) even under these conditions. Moreover, the line current is cycle-by-cycle-controlled due to the peak-current-mode control, and hence, the input-current feedback loop is extremely fast, thereby allowing this type of control to be used with high-frequency lines (above 400 Hz).

Index Terms—AC/DC converters, converters for lighting, current-mode control, high brightness (HB) LEDs, single-phase power factor (PF) correction.

I. INTRODUCTION

HIGH-BRIGHTNESS (HB) LEDs are very attractive light sources due to their excellent characteristics (high efficiency and longevity, and low–maintenance requirements) [1]. As they must be driven from a dc source, many types of power switching converter can be used to adapt primary energy sources to the requirements of HB LEDs [2]. Many authors have proposed different dc–dc converter topologies based on traditional dc–dc switching power converters [3]–[5]. However, while dc–dc converters are typically designed to control their output voltages, HB LEDs require a controlled output current.

On the other hand, if the primary energy source is the ac line, then some type of ac–dc converter must be placed between the line and the HB LEDs [6], [7]. It is known that, if the total power handled by these converters is greater than 25 W, then the low-frequency harmonic content of the line current must comply with specific regulations. For lighting equipment, the most widely used standard is EN 61000-3-2, Class C [8]. This class establishes a very strict harmonic content, such that only very sinusoidal line waveforms are able to comply with the aforementioned regulation. Therefore, the only practical method to comply with the EN 61000-3-2 Class C regulation is to use active high-power-factor (PF) converters, commonly called power factor correctors (PFCs).

In the next section, we will review three of the most popular control methods for PFCs, which are potential candidates to control PFCs driving HB LEDs.

A. Voltage-Follower Control [9]–[15]

A very simple solution providing an almost sinusoidal (in the case of the boost converter [11]) or completely sinusoidal (in the case of the flyback family of converters: buck–boost, flyback, SEPIC, Cuk and Zeta [12]–[15]) line current waveform consists of designing the topology to always operate in the discontinuous conduction mode (DCM). In this case, only one voltage feedback loop [see Fig. 1(a)] is needed to control the converter, and any conventional switching-mode power supply controller can be used for this purpose. Accordingly, the control circuitry is extremely simple.

The main drawback of this control strategy is that the design to operate in DCM at full load causes higher losses than the design to operate in continuous conduction mode (CCM). Hence, the converter efficiency becomes clearly lower.

B. Analog-Multiplier-Based Control [9], [10], [16]

The classical method to obtain a perfectly sinusoidal line waveform consists of using a control strategy based on two feedback loops, one input-current feedback loop and an output-voltage feedback loop. Furthermore, an analog multiplier must be used in the control circuitry [see Fig. 1(b)]. This option allows the converter to be designed to work in both modes of operation (DCM and CCM). By designing the converter to operate in CCM at heavy loads, the current stress is clearly less than in the case of operating in DCM at these loads, and hence, efficiency is higher.

The main disadvantage of this option is the complexity of the control circuitry and its cost. Several controllers have been designed for this purpose, but they are not cheap, especially in comparison with standard controllers for switching-mode power supplies. Moreover, some authors have presented modified control strategies of the multiplier-based control in order to correct some drawbacks: slow output voltage response [17], [18],

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The authors are with the Universidad de Oviedo, Grupo de Sistemas Electrónicos de Alimentación (SEA), Gijón 33204, Spain (e-mail: gonzalezdiego@uniovi.es; sebas@uniovi.es; rodriguezalberto@uniovi.es; rodriguezmiguel.uo@uniovi.es; mmhernando@uniovi.es).

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Three of the most popular methods to control PFCs. (a) Voltage-follower control. (b) Analog-multiplier-based control. (c) One-cycle control.

C. One-Cycle Control [23]–[28]

In recent years, a number of authors have proposed different low-cost control strategies for PFCs operating in CCM [23]–[28]. The goal of these control strategies is to simplify the existing control circuitry based on an analog multiplier. This simplification makes sense in the case of relatively low-power applications, such as PFCs for many types of PC power supplies, electronic ballast, and battery chargers in the range of 100–500 W. Some PFC control strategies based on standard peak-current-mode control have been proposed (e.g., nonlinear-carrier control [23], [24]). However, the most significant one is the one-cycle control (OCC) technique. The OCC technique [25] was proposed in [26] and [27] to be used in PFCs [see Fig. 1(c)]. Using this control method, the PFC can operate in CCM without using either an analog multiplier or an input voltage sensor. These control techniques are focused in boost topology as first stage of high PF ac–dc power supplies because their implementation is quite simple [26], [28]. In these cases, only one signal integrator is needed, whose integrator time constant must match the switching period for proper operation [27], [28]. In the case of PFCs based on converters belonging to the flyback family (i.e., flyback, buck–boost, SEPIC, Cuk and Zeta), either two matched integrators or a current sensor with an integrator with reset must be used [27]. This fact makes this method more complex and less attractive in the case of the flyback family of PFCs. However, a topology belonging to the flyback family of converters and with galvanic isolation can be very attractive to design a low-cost complete power supply with high PF in the range of 100 W. One of the possible applications for this topology is the drive of HB LEDs.

A new low-cost control strategy for PFCs is presented in this paper. This control strategy is a simplification of the OCC and voltage-controlled compensation ramp (VCCR) control [29]. It allows the use of conventional peak-current-mode controllers for switching-mode power supplies to control PFCs operating in CCM [Fig. 2(a)]. Hence, both low cost (due to the controller used) and high efficiency (due to the CCM operation) are
achieved. Moreover, input current is cycle-by-cycle-controlled, and hence, the input-current feedback loop is extremely fast, thus allowing this type of control to be used with relatively high-frequency lines (clearly above 400 Hz). The price to pay for these advantages is the quality of the line waveform, which will be very sinusoidal at rated conditions (rated load and input voltage), but will be less sinusoidal when the load decreases. In fact, the line current waveforms using the proposed method are the same as those obtained using OCC or VCCR control at rated conditions, but they become more distorted at different conditions. However, this is not a major problem, since the regulations (especially the IEC-1000-3-2 Class C [8]) must be met only at rated load and because the line waveform maintains a very high PF under all operating conditions.

This control strategy will be applied to the boost PFC and flyback family of PFCs (i.e., flyback, buck–boost, SEPIC, Cuk and Zeta topologies). The implementation of the proposed control for the case of using a boost PFC to drive the HB LEDs does not require any change in the controller circuitry in comparison with the use of this same controller in standard dc–dc converters [Fig. 2(b)]. Also, only an appropriate choice of the compensation ramp at full load and an output-current feedback loop to
control the HB LED current are required. This compensation function must be a linear ramp. In the case of PFCs based on the flyback family of converters, a simple solution to obtain a sinusoidal input current is presented in this paper. This solution is based on the use of an exponential function instead of a linear one. An adequate choice of the exponential ramp shape minimizes the total harmonic distortion (THD). This exponential compensation ramp can be implemented very easily by connecting a resistor $R_f$ in parallel with the oscillator capacitor $C_f$ in Fig. 2(c].

II. USING THE PROPOSED CONTROL WITH BOOST PFCs

Fig. 3(a) shows the key waveforms with the control method proposed in this paper. As this figure shows, the converter duty cycle is determined by the instant when the voltage $v_{EA} - v_{ramp}$ equals the value $i_s R_s$ (with $i_s R_s$ being the voltage across the current sensor). This is the same situation as in the case of the conventional peak-current-mode control, where the converter duty cycle is determined by the instant when the voltage $i_s R_s + v_{ramp}$ equals the value $v_{EA}$. At rated load and rated input voltage, the compensation ramp must be chosen, as shown in Fig. 3(a): the ramp amplitude must be equal to the control voltage $v_{EA}$. When the converter operating conditions change (e.g., at medium load), the control waveforms become those shown in Fig. 3(b), where the value of the control voltage $v_{EA}$ has changed and the slope of the compensation ramp remains constant. If these waveforms are compared with those obtained using either OCC or VCCR control [29], the control waveforms under rated operating conditions are exactly identical [see Fig. 4(a)], whereas they are different under the remaining operating conditions, as shown in Fig. 4(b). In fact, the value of the control voltage $v_{EA}$ and the ramp amplitude must coincide when OCC or VCCR control have been used, which implies a more complex circuitry because of the need for a variable slope ramp.

The value of $i_s S_2$ (which is the transistor current just before it stops conducting) can be obtained easily from geometric relationships in Fig. 3(b)

$$i_{S_2} = \frac{V_{rP} \lambda - d}{R_s} \quad (1)$$

where $V_{rP}$ is the peak value (amplitude) of the compensation ramp and $\lambda$ is the relative value of the control voltage $v_{EA}$, i.e.,

$$\lambda = \frac{v_{EA}}{V_{rP}} \quad (2)$$

The remaining equations needed to study the converter operation depend on the conduction mode.

A. Operation in CCM

In this case, Faraday’s law applied to both the transistor and the diode conduction periods yields

$$v_g = Lf_s \frac{i_{S_2} - i_{S_1}}{d} \quad (3)$$

$$V_O - v_g = Lf_s \frac{i_{S_2} - i_{S_1}}{1 - d} \quad (4)$$

where $i_{S_1}$ is the transistor current when it starts conducting, $f_s$ is the switching frequency ($f_s = 1/T_s$), $v_g$ is the input voltage, and $V_O$ is the output voltage. From (1)–(4), the following can be obtained easily:

$$i_{S_2} = \frac{V_{rP} \left( \lambda - \frac{V_O - v_g}{V_O} \right)}{R_s} \quad (5)$$

$$i_{S_1} = \frac{V_{rP} \left( \lambda - \frac{V_O - v_g}{V_O} \right)}{R_s} - \frac{v_g (V_O - v_g)}{V_O Lf_s} \quad (6)$$

The value of the average inductor (and line) current $i_{gav}$ is

$$i_{gav} = \frac{i_{S_2} + i_{S_1}}{2} \quad (7)$$

and from (5)–(7), we obtain

$$i_{gav} = \frac{V_{rP}}{R_s} \left( \lambda - \frac{V_O - v_g}{V_O} \right) - \frac{v_g (V_O - v_g)}{2V_O Lf_s} \quad (8)$$

B. Operation in DCM

In this case, $i_{S_1}$ is always 0, and (3) and (4) become

$$v_g = Lf_s \frac{i_{S_2}}{d} \quad (9)$$

$$V_O - v_g = Lf_s \frac{i_{S_2}}{d} \quad (10)$$
where $d'$ is the quotient between the inductor demagnetizing time and the switching period. From (2) and (9), we can obtain

$$i_{S2} = \frac{\lambda V_p}{R_S (1 + (V_p L f_s / R_S v_g))}. \quad (11)$$

The value of $i_{gav}$ in this case is

$$i_{gav} = \frac{i_{S2}(d + d')}{2} \quad (12)$$

and from (9)–(12), we finally obtain

$$i_{gav} = \left(\frac{V_p \lambda}{R_S}\right)^2 \frac{V_O L f_s}{2(V_O - v_g)v_f \lambda} \times \frac{1}{(1 + (V_p L f_s / R_S v_g))^2}. \quad (13)$$

C. Boundary Between Both Conduction Modes

Two dimensionless parameters are defined to study the boundary between CCM and DCM

$$K = \frac{2L f_s V_p}{R_S V_g} \quad (14)$$

$$M = \frac{V_O}{V_g} \quad (15)$$

where $V_g$ is the peak value of the line voltage

$$v_g = V_g |\sin \omega_L t|. \quad (16)$$

Taking into account these parameters, the value of $i_{S1}$ in CCM, given by (6), can be rewritten as follows:

$$i_{S1} = \frac{V_O K}{2L f_s M} \left(\lambda - 1 - \left(\frac{2}{K - 1}\right) |\sin \omega_L t| - \frac{2(|\sin \omega_L t|^2)}{MK}\right). \quad (17)$$

This equation can again be rewritten as

$$i_{S1} = \frac{V_O K}{2L f_s M} (\lambda - \lambda_{crit}) \quad (18)$$

where the value of $\lambda_{crit}$ is

$$\lambda_{crit} = 1 + \left(\frac{2}{K - 1}\right) |\sin \omega_L t| - \frac{2(|\sin \omega_L t|^2)}{MK}. \quad (19)$$

Therefore, the converter will operate in CCM when $\lambda > \lambda_{crit}$, in DCM when $\lambda > \lambda_{crit}$, and just on the boundary between both modes when $\lambda = \lambda_{crit}$. At rated load and rated input voltage (i.e., $\lambda = 1$), the condition to operate in CCM becomes

$$K > 2(M - |\sin \omega_L t|). \quad (20)$$

When the PFC is designed to operate in CCM for the entire line angle ($\omega_L t$) at rated load and rated input voltage (i.e., $\lambda = 1$), (20) becomes

$$K > 2M. \quad (21)$$

However, the situation is more complex for any $\lambda < 1$. In this case, the maximum converter duty cycle is limited by the control strategy, as shown in Fig. 5. Therefore, the converter cannot work in CCM for the entire line angle, irrespective of the value of $M$ and $K$. This fact is also illustrated in Fig. 6, where the values of $\lambda_{crit}$ have been plotted for different values of $K$

$$\lambda_{crit} = 1 + \left(\frac{2}{K - 1}\right) |\sin \omega_L t| - \frac{2(|\sin \omega_L t|^2)}{MK}. \quad (22)$$

Therefore, the converter operates in both modes (a part of the line angle, near the zero crossing, in DCM and a part of the line angle, near the peak value, in CCM) if $1 > \lambda > \lambda_{crit, min}$ and only in DCM if $\lambda < \lambda_{crit, min}$. Fig. 7(a) shows the normalized line current waveforms for different load conditions, while the same waveforms are given in Fig. 7(b) for different values of the line voltage. As this figure shows, the operation with values of $\lambda$ greater than 1 is possible. The control waveforms corresponding to this case are shown in Fig. 8(a) and the line current in a complete line cycle is given in Fig. 8(b). As this figure shows, the line current exhibits crossover distortion. This distortion is due to the fact that the line current in a half cycle never decreases to 0, as shown in Fig. 8(a). Only when the line voltage crosses 0, the line current rapidly changes its sign, causing the aforementioned distortion.

Finally, the PF and the THD for several design conditions are given in Fig. 9. This figure shows excellent values of PF and THD around the rated operating point (THD less than 5% and PF greater than 0.99 for $\lambda = 1$).

III. USING THE PROPOSED CONTROL WITH THE FLYBACK FAMILY OF PFCs

A. Use of an Exponential Compensation Ramp

As in the case of the boost PFC, the proposed control method for the flyback family of converters coincides with OCC and VCCR control at rated conditions ($\lambda = 1$). Therefore, the input
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Fig. 7. (a) Normalized line current for different values of $\lambda$. In this design, the power is 66% of the rated power when $\lambda = 0.8$, 36% when $\lambda = 0.6$, and 13% when $\lambda = 0.4$. (b) Normalized line current for different line voltages, from 20% less than the rated value ($\lambda = 1.116$) to 20% higher ($\lambda = 0.883$).

Fig. 8. (a) Main control waveforms and (b) line current when $\lambda > 1$, i.e., $v_{EA} > V_{rP}$.

Fig. 9. (a) PF and (b) THD for different possible designs.

Fig. 10. (a) Line waveforms of flyback family of PFCs operating in CCM at rated input voltage and full load with linear compensation ramp. (b) PF and THD values as a function of $M/n$.

Fig. 11. Main control waveforms with the proposed control and exponential compensation ramp (a) under nominal conditions, (b) under light load, and (c) when the line voltage is low.

The remaining equations needed to study the converter operation depend on the conduction mode.

B. Operation in CCM

In this case, (3) is also valid, and (4) and (7) become

$$V_O = nLf_S \frac{i_{S2} - i_{S1}}{1 - d}$$  \hspace{1cm} (25)

$$i_{gav} = \frac{i_{S2} + i_{S1}}{2} d$$  \hspace{1cm} (26)
and from (2), (24), (25), and (26), we obtain

$$i_{gav} = \frac{V_O}{V_O + \nu g} \left[ \frac{V_L}{R_S} \left( \lambda - \frac{1 - e^{-\left(V_O/(V_O + \nu g)\right)\mu}}{1 - e^{-\mu}} \right) \right]$$

$$i_{s1} = \frac{V_L}{R_S} \left( \lambda - \frac{1 - e^{-\left(V_O/(V_O + \nu g)\right)\mu}}{1 - e^{-\mu}} \right) - \frac{V_O \nu g}{L f_S (V_O + \nu g)} \right]$$

(27)

(28)

C. Boundary Between Both Conduction Modes

Following the same process as that followed in the case of the boost PFC, we obtain

$$\lambda_{crit} = \frac{2 M \sin \omega_L t}{K (M + n \sin \omega_L t)} + \frac{1 - e^{-\mu M/(M+n)\sin \omega_L t)}}{1 - e^{-\mu}}.$$

(29)

Therefore, the converter will operate in CCM when $\lambda > \lambda_{crit}$, in DCM when $\lambda < \lambda_{crit}$, and just on the boundary between both modes when $\lambda = \lambda_{crit}$. At the rated load and input voltage (i.e., $\lambda = 1$), the condition to operate in CCM becomes

$$K > K_{crit} = \frac{2 M \sin \omega_L t}{(M + n \sin \omega_L t)} \cdot \frac{1 - e^{-\mu}}{e^{-\mu} M/(M+n)\sin \omega_L t)} - \frac{1 - e^{-\mu}}{1 - e^{-\mu}}.$$

(30)

To guarantee CCM for the entire line period under these conditions, $K$ must be greater than the maximum value of $K_{crit}$. This maximum value occurs at $\omega_L = 0$ and, therefore, (30) becomes

$$K > K_{crit_{max}} = \frac{2 M (1 - e^{-\mu})}{n \mu e^{-\mu}}.$$  

(31)

Taking into account (31), $K$ can be expressed as

$$K = \alpha K_{crit_{max}} = \alpha \frac{2 M (1 - e^{-\mu})}{\mu e^{-\mu}}$$

(32)

where $\alpha$ is a design parameter that must be greater than 1 to guarantee CCM for the entire line period at rated conditions.

As (27) shows, the line current waveform depends on the value of $\mu$. Fig. 12(a) shows the waveforms in CCM for several values of $\mu$ and the same values of $M/n$ and $\alpha$ (i.e., $M/n = 0.7$, $\alpha = 2$). The THD obtained for a given value of $\alpha$ and different values of $M/n$ and $\mu$ is shown in Fig. 12(b). The value of $\mu$ that optimizes the THD for several design cases was obtained using a Mathcad spreadsheet. The results are shown in Fig. 12(c).

Moreover, taking into account the definition of $M$ [see (15)] and $\alpha$ [see (32)], (27) can be rewritten as follows:

$$i_{gav} = \frac{M}{M + n \sin \omega_L t} \times \frac{V_L}{R_S} \times \frac{1}{1 - e^{-\mu}}$$

$$\times \left( \lambda - 1 - \alpha e^{-\mu} + e^{-\mu} M/(M+n) \sin \omega_L t \right) - \frac{n \mu e^{-\mu}}{2 \alpha}.$$  

(33)

As a conclusion, the value of $\mu$ can be chosen in order to minimize THD under rated conditions ($\lambda = 1$), which are the conditions required to comply with regulations (i.e., EN 61000-3-2).

To study the conduction mode for any value of $\lambda$, the values of $\lambda_{crit}$ that defines operation points different to the rated ones are plotted in Fig. 13. As this figure shows, the minimum value of $\lambda_{crit}$ occurs at $\pi/2$ and its value is

$$\lambda_{crit_{min}} = \frac{2 M}{K (M + n)} + \frac{1 - e^{-\mu M/(M+n)}}{1 - e^{-\mu}}.$$  

(34)

As in the case of the boost PFC with the proposed control, the converter operates in both modes (a part of the line angle, near the zero crossing, in DCM and a part of the line angle, near the peak value, in CCM) if $1 > \lambda > \lambda_{crit_{min}}$ and only in DCM if $\lambda < \lambda_{crit_{min}}$.
Fig. 13. Values of $\lambda_{\text{crit}}$ for different designs.

Fig. 14. (a) Normalized line current for different values of $\lambda$. In this design, the power is 63.7% of the rated power when $\lambda = 0.98$, 36.5% when $\lambda = 0.96$, 15.7% when $\lambda = 0.94$, and 6.1% when $\lambda = 0.92$. (b) Normalized line current for different line voltages, from 20% less than the rated one ($\lambda = 1.0144$) to 20% higher ($\lambda = 0.9905$).

D. Operation in DCM

In this case, (9) and (24) are valid, and (10) and (12), respectively, become

$$V_O = n L f_s \frac{i_S d}{\omega_L}$$

$$i_{\text{gav}} = \frac{i_S d}{2}.$$  

E. Operation in Conditions Different From the Rated Ones

The set of equations (9), (24), (35), and (36) allows us to calculate $i_{S2}$, $i_{S1}$, and $i_{\text{gav}}$ in this case. From (9) and (24), we obtain a transcendental equation that must be numerically solved.

Fig. 14(a) shows the normalized line current waveforms for different load conditions, whereas the same waveforms are given in Fig. 14(b) for different values of the line voltage. In all these cases, the value of $\mu$ has been chosen to minimize the THD under nominal conditions, i.e., according to the curves plotted in Fig. 12(c). Finally, the PF and the THD for several design conditions are given in Fig. 15. This figure shows excellent values of PF and THD around the rated operating point (i.e., $\lambda = 1$). It should be noted that the converter must comply with the regulations under rated operating conditions. In this case, the results are very good (theoretical values of THD less than 2% and PF greater than 0.999 for $\lambda = 1$).

IV. Design Procedure for a Flyback Family of PFCs

The design procedure of a flyback PFC for driving HB LEDs using the proposed control is given in this section. The inputs of this design are the output voltage $V_O$, the peak value of the input voltage $V_{gP}$, and the power processed $P_g$. From these inputs, the peak value of the line current $i_{gP}$ can be calculated easily from the power balance, i.e., $i_{gP} = 2P_g/V_{gP}$. The steps can be summarized as follows.

Step 1: Calculate $M$ from (15) and choose $n$ according to a tradeoff between current and voltage stress in both the power transistor and diode. As in any PFC in CCM, the minimum duty cycle (corresponding to the peak value of the input voltage and current) should be around 50%, which means a reasonable tradeoff between voltage and current stress in the aforementioned power devices.

Step 2: Choose the value of $\alpha$. This value should be selected greater than 1, which guarantees CCM for the entire line angle at rated conditions. Once $M/n$ and $\alpha$ are known, determine the value of $\mu$ according to the plot given in Fig. 12(c).

Step 3: Calculate the value of the quotient $V_{rP}/R_S$. For this purpose, a perfect sinusoidal line waveform is assumed, which is a reasonable approach when the right value of $\mu$ has been chosen. Thus, the value of $i_{\text{gav}}$ at $\omega_L t = \pi/2$ and full load (i.e., $\lambda = 1$) obtained from (33) must be equal to the value of $i_{gP}$ calculated from the power balance. From this equality, the value of the quotient $V_{rP}/R_S$ can be calculated easily. To make this calculation even easier, a plot of $i_{gP} R_S/V_{gP}$ as a function of $M/n$ and $\alpha$ is given in Fig. 16. Once the value of $V_{rP}/R_S$ has been calculated, the individual values of $V_{rP}$ and $R_S$ can be chosen freely, but taking into account that they must be compatible with the controller voltage levels.

Step 4: Calculate the value of the flyback inductance $L$. Once the value of the quotient $V_{rP}/R_S$ is known, the value of $L$ can be calculated easily from the definitions of $K$ (14), $K_{\text{crit max}}$ (31), and $\alpha$ (32).

V. Experimental Results

A prototype of a flyback PFC to drive HB LEDs was built and tested. It was controlled by the proposed control strategy, which was implemented using a low-cost current-mode controller (UC3843). The circuit has been performed according to
the general scheme given in Fig. 2(c), where the output current is controlled (instead of the output voltage). The converter output is connected to four strings of four HB LEDs LXX2PW14T00 (Luxeon). A simple resistor (1 Ω/2 W) has been used to equalize the current of each string (Fig. 17). This method of driving multiple strings of HB LEDs introduces additional power losses. In order to solve this drawback, other equalization methods [30] can be used. It should be noted that the converter has not been designed for dimming. The rated operating conditions of this converter are: \( v_{gRMS} = 110 \, \text{V}, I_O = 3 \, \text{A}, P_g = 45 \, \text{W}, V_O = 14–16 \, \text{V}, n = 0.1, L = 1.15 \, \text{mH}, \) and \( f_s = 80 \, \text{kHz}. \) The design parameters of this setup are \( \alpha = 1.25 \) and \( \mu = 4.5. \) A more detailed diagram of the control circuitry is shown in Fig. 17. The values of the resistors \( R_{\text{ramp1}}, R_{\text{ramp2}}, \) and \( R_{\text{ramp3}} \) and the capacitor \( C_{\text{ramp}} \) have been chosen in order to generate an adequate compensation ramp \( (V_{rp} = 2.5 \, \text{V}) \) to minimize the THD of the input current. The values of the \( R_D, R_F, R_{\text{CL1}}, \) and \( R_{\text{CL2}} \) and the values of \( C_F, C_{\text{CL1}}, \) and \( C_{\text{CL2}} \) complete the output-current-feedback loop design, which depends on the IC used. Finally, resistors \( R_{11}, R_{12}, R_{1}, \) and \( R_{2} \) complete the IC design in order to adapt the control signals.

The control circuitry has been designed to obtain the higher PF value just when the converter starts working (HB LEDs at room temperature). Fig. 18 shows the evolution of the PF and of the HB LEDs temperature (measured on the heatsink at 6 mm from one HB LED lead) during the warm-up process. As this figure shows, the final operation temperature is reached after 1 h of operation. During the warm-up process, the voltage across the HB LEDs becomes lower and, therefore, the power handled by the converter decreases. Due to the very simple control circuitry proposed, the line current becomes slightly distorted when the HB LEDs reach their steady-state temperature. This fact is reflected in the evolution of the PF, which changes from 0.995 (at the beginning of the warm-up process) to 0.989 (at the end of this process). The harmonic content in the worst case is shown in Fig. 19, where it is compared with the limits imposed by the EN 61000-3-2 regulation in Class C. As this figure shows, the prototype complies with the aforementioned regulations. Moreover, Fig. 20 shows the line current waveforms corresponding to the beginning and the end of the warm-up process.

The operation at steady-state temperature for different line voltages around the nominal value (110 V) is shown in Fig. 21. When the line voltage is below or above its nominal value, the
The line waveform obtained is slightly distorted when the converter works under either overvoltage or undervoltage conditions (the PF measured in the prototype was always greater than 0.95). Moreover, excellent results were obtained when the line frequency is increased from 60 up to 800 Hz (PF measured always greater than 0.99 under nominal conditions). This is due to the fact that the line current is cycle-by-cycle-controlled, and hence, the input-current feedback loop is extremely fast.

Finally, the effect of the output voltage ripple on the converter operation has been studied. For a given load, this ripple depends on the capacitance of the bulk capacitor $C_B$. This capacitance has been varied from 30 (0.8 $V_{pp}$ ripple at 60 Hz) to 1 mF (3.8 $V_{pp}$ ripple at 60 Hz) and no appreciable flicker has been detected. The only consequence of increasing $C_B$ is the slight raise that the steady-state temperature suffers (from 88.2 $^\circ$C to 92.1 $^\circ$C).

VI. CONCLUSION

The control strategy presented here is extremely simple because it is based on the use of a conventional peak-current-mode controller for dc–dc converters, with no additional components. It only requires a special selection of the compensation slope waveform. In the case of the boost PFC, an almost perfect sinusoidal line current is obtained at full load using the standard linear compensation ramp. However, the line current waveform would be notably distorted if a linear compensation ramp were used in the case of flyback, buck–boost, SEPIC, Cuk or Zeta PFCS. To avoid this problem, an exponential waveform can be used in these cases as the compensation ramp. The time constant of this waveform can be chosen to minimize the THD. Its value is around four to five times greater than the switching period for many standard designs. Due to its simplicity and low cost, this control strategy is attractive to supply HB LED from an ac source.


Diego González Lamar (M’05) was born in Zaragoza, Spain, in 1974. He received the M.Sc. and Ph.D. degrees in electrical engineering from the Universidad de Oviedo, Gijón, Spain, in 2003 and 2008, respectively.

In 2003, he became a Research Engineer at the University of Oviedo and since September 2005, he has been an Assistant Professor. His research interests include switching-mode power supplies, converter modeling, and power-factor-correction converters.

Javier Sebastián Zúñiga (M’87) was born in Madrid, Spain, in 1958. He received the M.Sc. degree from the Polytechnic University of Madrid, Madrid, and the Ph.D. degree from the University of Oviedo, Gijón, Spain, in 1981 and 1985, respectively.

He was an Assistant Professor and an Associate Professor at both the Polytechnic University of Madrid and at the University of Oviedo. Since 1992, he has been with the University of Oviedo, where he is currently a Professor. His research interests include switching-mode power supplies, modelling of dc-to-dc converters, low output voltage dc-to-dc converters, and high power-factor rectifiers.

Alberto Rodríguez Alonso was born in Oviedo, Spain, in 1981. He received the M.S. degree in telecommunications engineering in 2006 from the University of Oviedo, Gijón, Spain, where he is currently working towards the Ph.D. degree (granted by the Spanish Ministry of Science and Education under the FPU program).

In 2006, he has been a Telecommunications Engineer with the Government of the Principality of Asturias and an Assistant Professor with the Department of Electrical Engineering, University of Oviedo. Since 2007, he has been working in the University of Oviedo at full time. His research interest is focused on bidirectional DC-DC power converters.

Miguel Rodríguez González (S’06) was born in Gijón, Spain, in 1982. He received the M.S. degree in telecommunication engineering from the University of Oviedo, Gijón, in 2006. He is currently working toward the Ph.D. degree in the Department of Electrical and Electronic Engineering, also at the University of Oviedo (granted by the Spanish Ministry of Science and Education under the FPU program).

His research interests include dc/dc conversion, high frequency power conversion, and power supply systems for RF amplifiers.

Marta María Hernando Álvarez (M’94) was born in Gijón, Spain, in 1964. She received the M.S. and Ph.D. degrees in electrical engineering from the University of Oviedo, Gijón, in 1988 and 1992, respectively.

She is currently an Associate Professor at the University of Oviedo. Her research interests include switching-mode power supplies and high-power-factor rectifiers.